Rockchip RK3128 Datasheet

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Revision History

Date	Revision	Description
2014-06-12	0.1	Initial Release
2014-07-09	0.2	Correction
2014-07-31	0.4	Update package information
2014-08-15	0.6	Correction layout

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Chapter 1 Introduction

RK3128 is a high performance Quad-core application processor for smart TV-Box. Especially it is a high-integration and cost efficient SOC for 1080P H.265 TV-Box.

Quad-core Cortex-A7 is integrates with separately Neon and FPU coprocessor, also shared 256KB L2 Cache. Mali400 MP2 GPU is embedded to support smoothly high-resolution (1080p) display and mainstream game.

Lots of high-performance interface to get very flexible solution, such as multi-pipe display with HDMI1.4, TV Encoder. Crypto hardware is integrated for support security BOOT. 32bits DDR3/LPDDR2 provides high memory bandwidths for high-performance.

HEVC hardware is integrated for support 1080P H.265 video.

1.1 Features

1.1.1 Microprocessor

- Quad-core ARM Cortex-A7MP Core processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Separately Integrated Neon and FPU per CPU
- 32KB/32KB L1 I-Cache/D-Cache per CPU.
- Unified 256KB L2 Cache.

1.1.2 Memory Organization

- Internal on-chip memory
  - 16KB BootRom
  - 8KB internal SRAM
- External off-chip memory①
  - DDR3-1066/DDR3L-1066, 32bits data width, 2 ranks, totally 2GB(max) address space
  - LPDDR2-800, 32bits data width, 2 ranks, totally 2GB(max) address space
  - Async/Toggle/SyncNand Flash(include LBA Nand), 8bits data width,4 banks, 60bits ECC

1.1.3 Internal Memory

- Internal BootRom
  - Size : 16KB
  - Support system boot from the following device :
    - 8bits Async Nand Flash
    - 8bits toggle Nand Flash
    - SPI interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface

- Internal SRAM
  - Size : 8KB

1.1.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/LPDDR2)
  - Compatible with JEDEC standard DDR3/DDR3L/LPDDR2 SDRAM
  - Data rates up to 1066Mbps(533MHz) for DDR3/DDR3L/LPDDR2
  - Supports 2 ranks (chip selects), totally 2GB (max) address space.
  - 7 host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR2 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/LPDDR2 SDRAM; clock stop and deep power-down for LPDDR2 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation

- Nand Flash Interface
  - Support 8bits async/toggle/syncnandflash, up to 4 banks
  - Support LBA nandflash
  - 16bits, 24bits, 40bits, 60bits hardware ECC
  - For DDR nandflash, support DLL bypass and 1/4 or 1/8 clock adjust
  - For async/togglenandflash, support configurable interface timing, maximum data rate is 16bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method
  - Also support data transfer by AHB slave interface together with external DMAC

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.5 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD2.0, MMC ver 4.5
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate

- Support block size from 1 to 65535Bytes
- Data bus width is 4bits

1.1.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3128
  - One oscillator with 24MHz clock input and 4 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatically clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 2 separate voltage domains
  - 3 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 6 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with four 64-bits AXI masters, one 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves

- Display interconnect with three 128-bits AXI master, four 64-bits AXI masters and one 32-bits AHB slave
- GPU interconnect with one 128-bits AXI master with point-to-point AXI-lite architecture and 32-bits APB slave
- VCODEC interconnect also with two 64-bits AXI master and two 32-bits AHB slave, they are point-to-point AXI-lite architecture

- Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 74 SPI interrupt sources input from different components inside RK3128
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ)separatelyfor each Cortex-A7, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - One embedded DMA controller PERI_DMAC for peripheral system
  - PERI_DMAC features:
    - 8 channels totally
    - 16 hardware request from peripherals
    - 2 interrupt output
    - Not support trustzone technology

- Security system
  - Embedded encryption and decryption engine
    - Support AES 128/192/256 bits key mode, ECB/CBC/CTR chain mode, Slave/FIFO mode
    - Support DES/3DES (ECB and CBC chain mode) , 3DES (EDE/ EEE key mode), Slave/FIFO mode
    - Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only
    - Support 160 bit Pseudo Random Number Generator (PRNG)
    - Support PKA 512/1024/2048 bit Exp Modulator

1.1.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Embedded memory management unit(MMU)

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264, H.265,VC-1, RV, VP6/VP8, Sorenson Spark, MVC
  - MMU Embedded
  - Supports frame timeout interrupt , frame finish interrupt and bitstream error interrupt
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.265 up to MP Level 4.1 High Tier : 1080P@60fps
  - H.264 up to HP level 4.2 : 1080p@60fps
  - MPEG-4 up to ASP level 5 : 1080p@60fps
  - MPEG-2 up to MP : 1080p@60fps
  - MPEG-1 up to MP : 1080p@60fps
  - H.263 : 576p@60fps
  - Sorenson Spark : 1080p@60fps
  - VC-1 up to AP level 3 : 1080p@30fps
  - RV8/RV9/RV10 : 1080p@60fps
  - VP6/VP8 : 1080p@60fps
  - MVC : 1080p@60fps
  - For H.264, image cropping not supported
  - For MPEG-4,GMC(global motion compensation)not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 UP to HP@level4.1, MVC and VP8
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 1920x1080 @ 25FPS[8]

1.1.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate[4] is up to 76million pixels per second

- Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate④ up to 90million pixels per second
  - Embedded memory management unit(MMU)

1.1.8 Image Enhancement (IEP module)

- Image format support
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - ARGB/XRGB/RGB565/YUV swap
  - UV SP/P
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - RGB dither up/down
  - YUV up/down sampling
  - Max source image resolution: 8192x8192
  - Max scaled image resolution: 4096x4096

- YUV enhancement
  - Hue, Saturation, Brightness, Contrast adjustment

- RGB enhancement & denoise
  - Contrast enhancement
  - Color enhancement
  - Gamma adjustment

- High quality scale
  - Averaging filter down-scaling
  - Bi-cubic up-scaling
  - Arbitrary non-integer horizontal & vertical scaling ratio range from 1/16 to 16

- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 1920
  - Configured high frequency de-interlace
  - I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode

- Interface
  - Configured direct path to LCDC if source width no more than 1920
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

1.1.9 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 32KB size
- 2D Graphics Engine(RGA module) :
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, and pattern mask
  - 8K x 8K raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Programmable bicubic filter to support image scaling
  - Blending, scaling and rotation are supported in one pass for stretch blit
  - Source formats :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
    - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.1.10 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support image crop with arbitrary windows
- Display Interface
  - Support HDMI 1.4 output up to 1080P@60Hz
  - TV Interface: ITU-R BT.656(8-bit, 480i/576i/1080i),TV encoder 10bit out for DAC, RGB888+1080i for HDMI, Parallel RGB HDMI interface:24-bit(RGB888 YCbCr444)
  - Max output resolution 1920x1080 for HDMI, 480i/576i for CVBS
  - 4 display layers :

- One background layer with programmable 24bits color
- One video layer (win0)
  - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
  - maximum resolution is 1920x1080,support virtual display
  - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
  - 256 level alpha blending(pre-multiplied alpha support)
  - Support transparency color key
  - De-flicker support for interlace output
  - Direct path support
  - YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)
  - RGB2YCbCr(BT601/BT709)
- One video layer (win1)
  - RGB888, ARGB888, RGB565
  - Support virtual display
  - 256 level alpha blending (pre-multiplied alpha support)
  - Support transparency color key
  - Direct path support
  - RGB2YCbCr(BT601/BT709)
- Hardware cursor(win3)
  - 8BPP (ARGB888 LUT)
  - Support two size: 32x32 and 64x64
  - 256 level alpha blending
  - Support hwc over panel at right and below side

- Win0 and Win1 layer overlay exchangeable
- 3 x 256 x 8 bits display LUTs
- Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
- Blank and blank display
- Scaler
  - Output for RGB (max up to 1024x768), not support interlace

1.1.11 HDMI

- HDMI version 1.4a, HDCP revision 1.4 and DVI version 1.0 compliant transmitter
- Supports DTV from 480i to 1080i/p HD resolution
- Supports 3D function defined in HDMI 1.4 spec
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug

1.1.12 Audio Interface

- I2S/PCM with 8ch
  - Up to 8 channels (8xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- I2S/PCM with 2ch
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

- Audio Codec
  - Digital interpolation and decimation filter integrated
  - Line-in, Microphone in and Speaker out Interface
  - On-Chip Analog Post Filter and digital filters
  - Single–ended or differential Input and Output
  - Sampling Rate of 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz
  - Support 16ohm to 32ohm Head Phone and Speaker Phone Output
  - Mono, Stereo channel supported
  - Optional Fractional PLL available that support 6Mhz to 20Mhz clock input to any clock output that meets 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz and 128 time oversampling ratio.

1.1.13 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- High-speed ADC stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface

- TS interface
  - Supports one TS input channel.

- Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
- Supports 2 TS sources: demodulators and local memory.
- Supports 1 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
  - 64 PID filters.
  - TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps
  - 16 PES/ES filters with PTS/DTS extraction and ES start code detection.
  - 4 PCR extraction channels
  - 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
  - PID done and error interrupts for each channel
  - PCR/DTS/PTS extraction interrupt for each channel
- 1 built-in multi-channel DMA Controller.

- Smart Card
  - support card activation and deactivation
  - support cold/warm reset
  - support Answer to Reset (ATR) response reception
  - support T0 for asynchronous half-duplex character transmission
  - support T1 for asynchronous half-duplex block transmission
  - support automatic operating voltage class selection
  - support adjustable clock rate and bit (baud) rate
  - support configurable automatic byte repetition

- GMAC 10/100/1000M Ethernet Controller
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
    - Supports IEEE 802.3x flow control for full-duplex operation
    - Optional forwarding of received pause control frames to the user application in full-duplex operation
    - Back-pressure support for half-duplex operation
    - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable InterFrameGap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP

checksum encapsulated in IPv4 or IPv6 datagrams
- Comprehensive status reporting for normal operation and transfers with errors
- Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
- Handles automatic retransmission of Collision frames for transmission
- Discards frames on late collision, excessive collisions, excessive deferral and underrun conditions

- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- UART Controller
  - 3 on-chip uart controller inside RK3128
  - DMA-based or interrupt-based operation
  - UART0 Embeddeds two 64Bytes FIFO for TX and RX operation respectively
  - UART1/UART2 Embedded two 32Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support auto flow control mode

- I2C controller
  - 4 on-chip I2C controller in RK3128
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3) , 32 GPIOs per group in GPIO0~GPIO3, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Embedded 1 USB Host 2.0 interfaces
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels

- Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.1.14 Others

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter
  - Sample rate Fs is 200KHz
  - SAR-ADC clock must be large than 11*Fs, recommend is 11*Fs
  - DNL is less than ±1 LSB , INL is less than ±2.0 LSB
  - Power supply is 3.3V (±10%) for analog interface, power dissipation is less than 900uW

- eFuse
  - Two high-density electrical Fuse is integrated: 512bits (64x8)
  - Support standby mode
  - Programming condition : VP must be 2.5V(±10%)
  - Program time is 2us.
  - Read condition: VP must be 0V or Floating.
  - Provide inactive mode, VP must be 0V or Floating in this mode.

- Operation Temperature Range
  - -40°C to +85°C

- Operation Voltage Range
  - IO supply : 3.3V (±10%)

- Package Type
  - BGA316 (body: 14mm x 14mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

- Power
  - TBA

Notes : ①: DDR3/LPDDR2/LPDDR3 are not used simultaneously as well as async and sync ddrnand flash

②: In RK3128, Video decoder and encoder are not used simultaneously because of shared internal buffer

③: Actual maximum frame rate will depend on the clock frequency and system bus performance

④: Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RK3128.

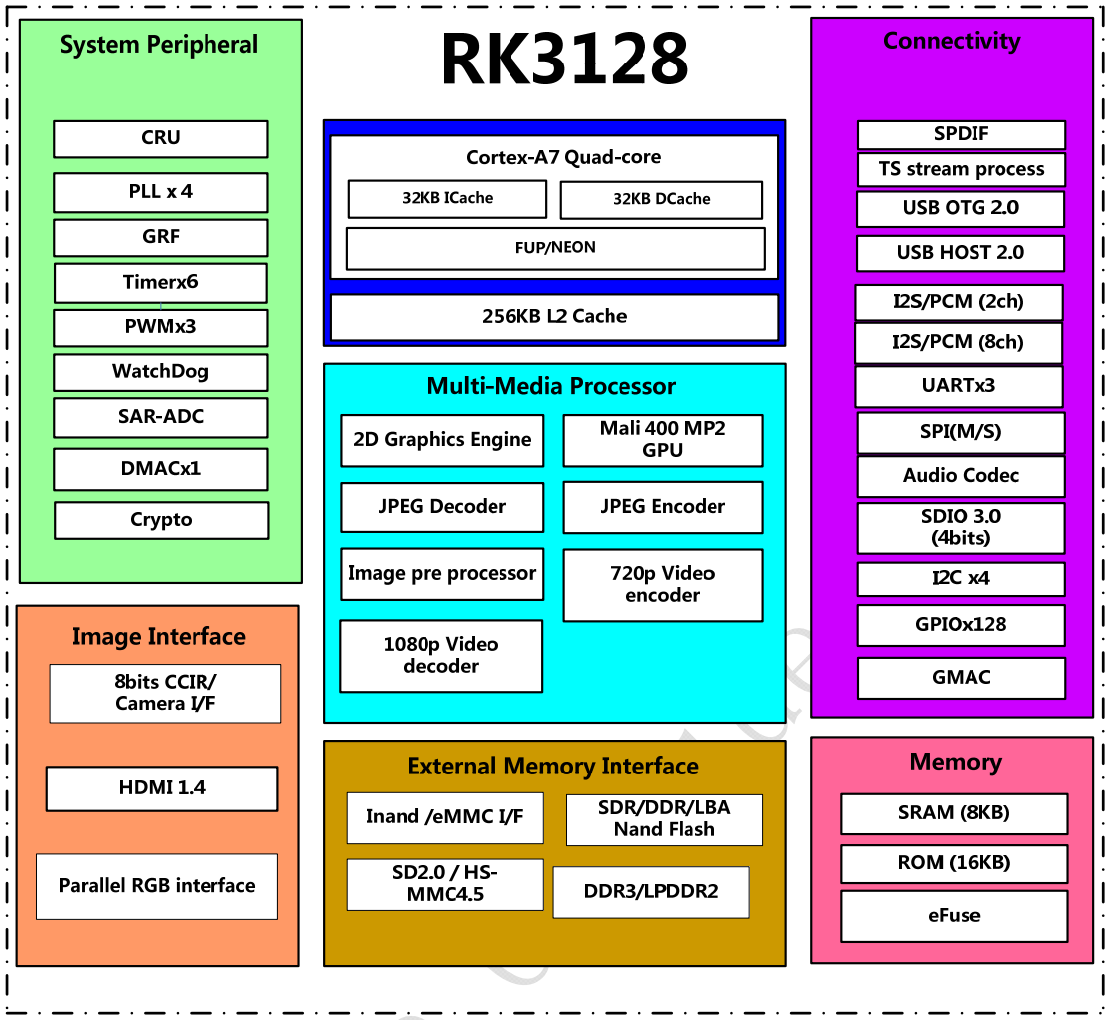


Fig.1-1RK3128 Block Diagram

1.3 Pin Description

In this chapter, the pin description will be divided into two parts, one is all power/ground descriptions in Table 1-1, include analog power/ground, another is all the function signals descriptions in Table 1-2, also include analog power/ground.

1.3.1 RK3128 power/ground IO descriptions

Table 1-1 RK3128 Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	B14, C3,C7,C10,C13, G3,G13, H8,H9,H10,H11,H12,H13, J8,J9,J10,J11,J12,J13, K3,K8,K9,K10,K11,K12,K13, L8,L9,L10,L11,L12,L13,L14 M2,M8,M9,M10,M11,M12,M13,	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground

	N7,N8,N9,N10,N11,N12,N13, P7,P8,V3,W6,W9,W12,W15				
AVDD	P12,P13,P14,N14,M14	1.08	1.2	1.32	Internal CPU Power (@ cpu frequency <= 1GHz)
CVDD	G7,K7,P10,J14,H14,G10	1.08	1.2	1.32	Internal Core Power
VCCIO1	N6	3	3.3	3.6	Digital GPIO Power
VCCIO2	T14	3	3.3	3.6	Digital GPIO Power
VCCIO3	K14	3	3.3	3.6	Digital GPIO Power
VCCIO4	G14	3	3.3	3.6	Digital GPIO Power
DDR_VDD	H7,J7,L7,M7,G12,G11,G9,G8	1.4 N/A	1.5 1.35	1.6 N/A	DDR3 Digital IO Power LVDDR3 Digital IO Power
A/GPLL_DVDD11	N3	0.99	1.1	1.21	ARM PLL Analog Power
C/DPLL_DVDD11	N4	0.99	1.1	1.21	DDR PLL Analog Power
PLL_VCCIO	N5	3	3.3	3.6	DDR PLL Analog Power
SAR_AVDD33	P9	2.97	3.3	3.67	SAR-ADC Analog Power
USB_DVDD11	T11	0.99	1.1	1.21	USB OTG2.0/Host 2.0 Digital Power
USB_AVDD33	T10	2.97	3.3	3.63	USB OTG2.0/Host 2.0 Analog Power
CODEC_AVDD	D13	2.97	3.3	3.63	Audio Codec Analog Power

CODEC_AVSS	D14				Audio Codec Analog Ground
HDMI_DVDD1V1_1	V4	0.99	1.1	1.21	HDMI Digital Power
HDMI_AVDD33	V2	3.0	3.3	3.6	HDMI Analog Power
TV ENCODER_AVDD	T7	2.97	3.3	3.63	TV ENCODER Analog Power
TV ENCODER_AGND	T8				TV ENCODER Analog Ground

1.3.2 RK3128 function IO descriptions

Table 1-2 RK3128 IO descriptions

Ball Name	Ball #	func1	func2	func3	func4	pad① type	Driving ②	Pull up /down	Reset State ③	power supply⑤
Left Side④										
DDR_A0	D1									
DDR_A2	E2									
DDR_A5	E5									
DDR_A9	E1									
DDR_A13	G1									
DDR_A7	E4									
DDR_ODT1	G2									
DDR_RESETN	F6									
DDR_DQ10	F2									
DDR_DQ8	G6									
DDR_DQS1	H1									
DDR_DQS1_N	H2									
DDR_DQ14	K2									
DDR_DQ12	H3									
DDR_DQ15	K1									
DDR_DQ13	J2									
DDR_DQ9	G5									
DDR_DM1	H4									
DDR_DQ11	H6									
DDR_DQ26	G4									
DDR_DQ24	K4									

DDR_DQS3	L1									
DDR_DQS3_N	L2									
DDR_DQ30	L5									
DDR_DQ28	H5									
DDR_DQ31	L6									
DDR_DQ29	K6									
DDR_DQ25	L4									
DDR_DM3	L3									
DDR_DQ27	K5									
XOUT24M	N1									
XIN24M	N2									
GPIO2_C6/LCDC_D20/EBC_BORDER0/GPS_SIGN/GMAC_TXD2	P5									
GPIO2_C7/LCDC_D21/EBC_BORDER1/GPS_MAG/GMAC_TXD3	P4									
GPIO2_C5/LCDC_D19/EBC_SDSHR/I2C2_SCL/GMAC_RXD2	P3									
GPIO2_C4/LCDC_D18/EBC_GDRL/I2C2_SDA/GMAC_RXD3	T4									
GPIO2_C3/LCDC_D17/EBC_GDPWR0/GMAC_TXD0	P2									
GPIO2_C2/LCDC_D16/EBC_GDSP/GMAC_TXD1	P1									
GPIO2_C1/LCDC_D15/EBC_GDOE/GMAC_RXD0	R2									
GPIO2_C0/LCDC_D14/EBC_VCOM/GMAC_RXD1	T3									
GPIO2_D1/LCDC_D23/EBC_GDPWR2/GMAC_MDC	T2									
GPIO2_D0/LCDC_D22/EBC_GD	P6									

PWR1/GPS_CLK/GMAC_COL										
GPIO2_B7/LCDC_D13/EBC_SDCE5/GMAC_RXER	T1									
GPIO2_B6/LCDC_D12/EBC_SDCE4/GMAC_CLK	U4									
GPIO2_B5/LCDC_D11/EBC_SDCE3/GMAC_TXEN	U2									
GPIO2_B4/LCDC_D10/EBC_SDCE2/GMAC_MDIO	U3									
GPIO2_B3/LCDC_DEN/EBC_GDCLK/GMAC_RXCLK	U1									
GPIO2_B2/LCDC_VSYNC/EBC_SDOE/GMAC_CRS	V5									
GPIO2_B1/LCDC_HSYNC/EBC_SDLE/GMAC_TXCLK	T5									
GPIO2_B0/LCDC_CLK/EBC_SDCLK/GMAC_RXDV	U5									
HDMI_EXTR	W3									
HDMI_TX3N	W1									
HDMI_TX3P	Y1									
HDMI_TX0N	W2									
HDMI_TX0P	Y2									
HDMI_TX1N	W4									
HDMI_TX1P	Y4									
HDMI_TX2N	W5									
HDMI_TX2P	Y5									
TV ENCODER_IOUTN	U7									
TV ENCODER_IOUTP	V7									
TV ENCODER_IREF	U8									

LVDS/MIPI_EXTR	V8									
LCDC_D9/LVDS_CLKN/EBC_SDCE1/MIPI_CLKN	W7									
LCDC_D8/LVDS_CLKP/EBC_SDCE0/MIPI_CLKP	Y7									
LCDC_D7/LVDS_TX3N/EBC_SDDO7/MIPI_D3N	Y8									
LCDC_D6/LVDS_TX3P/EBC_SDDO6/MIPI_D3P	W8									
LCDC_D5/LVDS_TX2N/EBC_SDDO5/MIPI_D2N	W10									
LCDC_D4/LVDS_TX2P/EBC_SDDO4/MIPI_D2P	Y10									
LCDC_D3/LVDS_TX1N/EBC_SDDO3/MIPI_D1N	W11									
LCDC_D2/LVDS_TX1P/EBC_SDDO2/MIPI_D1P	Y11									
LCDC_D1/LVDS_TX0N/EBC_SDDO1/MIPI_D0N	W13									
LCDC_D0/LVDS_TX0P/EBC_SDDO0/MIPI_D0P	Y13									
USB1_DP	W14									
USB1_DM	Y14									
USB_EXTR	V11									
USB0_VBUS	U11									
USB0_ID	R11									
USB0_DM	Y16									
USB0_DP	W16									
ADCIN0	P11									
ADCIN1	U10									

ADCIN2	V10									
EFUSE	R10									
EFUSE	R10									
CIF_D0/TS_D0	U17									
CIF_D1/TS_D1	V17									
CIF_D2/TS_D2	W17									
CIF_D3/TS_D3	V16									
CIF_D4/TS_D4	T13									
CIF_D5/TS_D5	R13									
CIF_D6/TS_D6	R14									
CIF_D7/TS_D7	T16									
CIF_VSYNC/TS_SYNC	U13									
CIF_CLKI/TS_VALID	U16									
CIF_HREF/TS_FAIL	V18									
GPIO3_C1/DRIVE_VBUS/PMIC_SLEEP	U14									
CIF_CLKO/TS_CLKO	V13									
GPIO0_D2/PWM0	U18									
CIF_PDN1/GPIO3_B3	Y20									
GPIO0_D3/PWM1	T17									
GPIO0_D4/PWM2	V14									
GPIO3_D2/IR	W18									
GPIO3_D3/SPDIF	Y19									
GPIO2_D2/CARD_RST/UART0_TX	T18									
GPIO2_D3/CARD_CLK/UART0_RX	Y17									
GPIO1_C1/SDMMC0_DET	W19									

GPIO2_D4										
GPIO2_D5/CARD_DET/UART0_CTSN	W20									
GPIO1_C6/FLASH_CS2/EMMC_CMD	U19									
GPIO2_A5/FLASH_WP/EMMC_PWR	V19									
GPIO1_C7/FLASH_CS3/EMMC_RST	P19									
GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0	P16									
GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2	T19									
GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1	U20									
GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3	T20									
GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD	P18									
GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0	N15									
GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD	R19									
GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1	P17									
GPIO2_A0/FLASH_ALE/SPI_CLK	N16									
GPIO2_A1/FLASH_CLE	N17									
GPIO2_A2/FLASH_WRN/SFC_CSN0	P20									

GPIO2_A3/FLASH_RDN/SFC_CSN1	L15									
GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_CLK	K17									
GPIO2_A6/FLASH_CS0	L16									
GPIO2_A7/FLASH_DQS/EMMC_CLKO	N19									
GPIO0_C7/FLASH_CS1	L17									
TEST	H15									
GPIO1_B6/SDMMC0_PWR	N18									
NPOR	N20									
GPIO1_C5/SDMMC0_D3/JTAG_TMS	M19									
GPIO1_C4/SDMMC0_D2/JTAG_TCK	K16									
GPIO1_C3/SDMMC0_D1/UART2_RX	K15									
GPIO1_C2/SDMMC0_D0/UART2_TX	L18									
GPIO1_A7/SDMMC0_WP	L19									
GPIO0_B6/I2S_SDI/SPI_CSN0	K19									
GPIO3_D7/CIF_PDN0/TEST_CLKO	K18									
GPIO0_B5/I2S_SDO/SPI_RXD	L20									
GPIO0_B4/I2S_LRCK_TX	H16									
GPIO0_B3/I2S_LRCK_RX/SPI_TXD	J19									
GPIO0_B1/I2S_SCLK/SPI_CLK	K20									
GPIO0_B0/I2S_MCLK	H17									
GPIO1_C0/SDMMC0_CLKO	H20									

GPIO1_B3/UART1_RTSN/SPI_CSN0	G18									
GPIO1_B2/UART1_RX/SPI_RXD	H19									
GPIO1_B1/UART1_TX/SPI_TXD	H18									
GPIO3_C0										
GPIO1_B0/UART1_CTSN/SPI_CLK	G19									
GPIO1_A5/I2S_SDI/SDMMC1_D3	G17									
GPIO1_A4/I2S_SDO/SDMMC1_D2	G16									
GPIO1_A3/I2S_LRCK_TX	G15									
GPIO1_A2/I2S_LRCK_RX/SDMMC1_D1	E19									
GPIO1_A1/I2S_SCLK/SDMMC1_D0/PMIC_SLEEP	E18									
GPIO1_A0/I2S_MCLK/SDMMC1_CLKO/XIN_32K	E20									
GPIO1_B7/SDMMC0_CMD	D18									
GPIO0_A3/I2C1_SDA/SDMMC1_CMD	D17									
GPIO0_A1/I2C0_SDA	E17									
GPIO0_A2/I2C1_SCL	F19									
GPIO0_A0/I2C0_SCL	D20									
GPIO0_C4/HDMI_CEC	C19									
GPIO0_B7/HDMI_HPD	E13									
GPIO0_A6/HDMI_SCL/I2C3_SCL	B20									
GPIO0_A7/HDMI_SDA/I2C3_SDA	F14									

GPIO3_C7	G20									
GPIO3_C6	C18									
GPIO3_C5	F13									
GPIO3_C4	D19									
GPIO3_C3										
GPIO3_C2										
GPIO1_B4/SPI_CSN1	B19									
GPIO0_D5										
GPIO0_D6/SDMMC1_PWR	A20									
GPIO0_D7										
GPIO0_D1/UART2_CTSN	A19									
GPIO0_D0/UART2_RTSN/PMIC_SLEEP	C17									
GPIO0_C6										
GPIO0_C3										
GPIO0_C2										
GPIO0_C1/CARD_IO/UART0_RTSN	P15									
GPIO0_C0										
GPIO3_D6										
GPIO3_D5										
GPIO3_D4										
GPIO3_D1										
CODEC_MICL	E14									
CODEC_AIL	C16									
CODEC_VCM	A17									
CODEC_MICBIAS	B18									
CODEC_AIR	D16									

CODEC_MICR	E16									
CODEC_AOL	B17									
CODEC_AOMS	A16									
CODEC_AOM	B16									
CODEC_HPDET	C14									
CODEC_AOR	B15									
DDR_DQ18	B9									
DDR_DQ16	A10									
DDR_DQS2	A11									
DDR_DQS2_N	B11									
DDR_DQ22	F10									
DDR_DQ20	E10									
DDR_DQ23	A13									
DDR_DQ21	B12									
DDR_DQ17	C11									
DDR_DM2	D11									
DDR_DQ19	E11									
DDR_DQ2	F11									
DDR_DQ0	A14									
DDR_DQS0	A8									
DDR_DQS0_N	B8									
DDR_DQ6	B13									
DDR_DQ4	B10									
DDR_DQ7	C8									
DDR_DQ5	D10									
DDR_DQ1	F8									
DDR_DM0	B7									
DDR_DQ3	A7									
DDR_A8	D8									

DDR_A6	F7									
DDR_A14	B5									
DDR_A15	A5									
DDR_A11	C5									
DDR_A1	A4									
DDR_A4	A2									
DDR_A12	B4									
DDR_BA1	E8									
DDR_BA0	D7									
DDR_A10	C4									
DDR_CKE	B3									
DDR_ODT0	B2									
DDR_CLK_N	C2									
DDR_CLK	B1									
DDR_RASN	E3									
DDR_CASN	E7									
DDR_CSN1	B6									
DDR_CSN0	A1									
DDR_WEN	D5									
DDR_BA2	D3									
DDR_A3	D2									

Notes :

① ：Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground, DP = Digital Power , DG = Digital Ground, A = Analog

②:Output Drive Unit is mA , only Digital IO have drive value

③:Reset state : I = input without any pull resistor ,O = output without any pull resistor ,

④:It is die location. For examples, “Left side” means that all the related IOs are always in left side of die

⑤:Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring

1.3.3 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 1-3 RK3128 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Power on reset for chip

Interface	Pin Name	Direction	Description
Debug	TCK	I	JTAG interface clock input/SWD interface clock input
	TMS	I/O	JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~3)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.
	sdmmc_write_prt	I	sdmmc card write protect signal, a 1 represents write is protected.
	sdmmc_rstn_out	O	sdmmc card reset signal
	sdmmc_pwr_en	O	sdmmc card power-enable control signal

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output.
	sdio_detect_n	I	sdio card detect signal, a 0 represents presence of card.
	sdio_write_prt	I	sdio card write protect signal, a 1 represents write is protected.
	sdio_pwr_en	O	sdio card power-enable control signal
	sdio_int_n	O	sdio card interrupt indication
	sdio_backend	O	the back-end power supply for embedded device

Interface	Pin Name	Direction	Description
eMMC	emmc_clkout	O	emmc card clock.

Interface	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.
	emmc_pwr_en	O	emmc card power-enable control signal
	emmc_rstn_out	O	emmc card reset signal

Interface	Pin Name	Direction	Description
DMC	CLK	O	Active-high clock signal to the memory device.
	CLK_N	O	Active-low clock signal to the memory device.
	CKE	O	Active-high clock enable signal to the memory device
	CSN*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASN	O	Active-low row address strobe to the memory device.
	CASN	O	Active-low column address strobe to the memory device.
	WEN	O	Active-low write enable strobe to the memory device.
	BAi(i=0,1,2)	O	Bank address signal to the memory device.
	Ai(i=0~15)	O	Address signal to the memory device.
	DQi(i=0~31)	I/O	Bidirectional data line to the memory device.
	DQS0 DQS1 DQS2	I/O	Active-high bidirectional data strobes to the memory device.
	DQS0_N DQS1_N DQS2_N	I/O	Active-low bidirectional data strobes to the memory device.
	DMi(i=0~3)	O	Active-low data mask signal to the memory device.
	ODT*i*(*i*=0,1)	O	On-Die Termination output signal for two chip select.
	RESETN	O	DDR3 reset signal to the memory device

Interface	Pin Name	Direction	Description
NandC	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal

	flash_data[*i*](*i*=0~7)	I/O	8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	flash_rdy	I	Flash ready/busy signal
	flash_csn*i*(*i*=0~3)	O	Flash chip enable signal for chip i, i=0~3

Interface	Pin Name	Direction	Description
I2S/PCM Controller (8 channel)	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock
	i2s_lrck_rx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdo	O	I2S/PCM serial data ouput
	i2s_lrck_tx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
SPI Controller	spi_clk	I/O	spi serial clock
	spi_csn*y* *(y=0,1)*	I/O	spi chip select signal,low active
	spi_txd	O	spi serial data output
	spi_rxd	I	spi serial data input

Interface	Pin Name	Direction	Description
LCDC	lcdc_dclk	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	lcdc_vsync	O	LCDC RGB interface vertival sync pulse, MCU i80 interface CSN signal
	lcdc_hsync	O	LCDC RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	lcdc_den	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	lcdc_data[23:0]	I/O	LCDC data output/input

Interface	Pin Name	Direction	Description
Camera IF	cif_clkin	I	Camera interface input pixel clock
	cif_clkout	O	Camera interface output work clock

	cif_vsync	I	Camera interface vertical sync signal
	cif_href	I	Camera interface horizontial sync signal
	cif_data[7:0]	I	Camera interface 8-bit input pixel data

Interface	Pin Name	Direction	Description
GPS	gps_sign	I	GPS sign data input
	gps_mag	I	GPS mag data input
	gps_clk	I	GPS rf clock input

Interface	Pin Name	Direction	Description
PWM	Pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock

Interface	Pin Name	Direction	Description
UART	uart0_sin	I	UART0 searial data input
	uart0_sout	O	UART0 searial data output
	uart0_cts_n	I	UART0 clear to send
	uart0_rts_n	O	UART0 request to send
	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_cts_n	O	UART1 clear to send
	uart1_rts_n	I	UART1 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output

Interface	Pin Name	Direction	Description
USB OTG2.0 /HOST 2.0	USB0PP	I/O	USB OTG 2.0 Data signal DP
	USB0PN	I/O	USB OTG 2.0 Data signal DM
	VBUS_0	N/A	USB OTG 2.0 5V power supply pin
	USB0ID	I	USB OTG 2.0 ID indicator
	otg_drv_vbus	O	USB OTG 2.0 drive VBUS
	USB1PP	I/O	USB HOST 2.0 Data signal DP
	USB1PN	I/O	USB HOST 2.0 Data signal DM
	VBUS_1	N/A	USB HOST 2.0 5V power supply pin

	USB1ID	I	USB HOST 2.0 ID indicator
	USBRBIAS	N/A	45 Ohm Reference external resistance

Interface	Pin Name	Direction	Description
Audio Codec	MICL	I	Left channel microphone PGA positive input
	LINEL	I	Left channel line-in input
	VCM	I	Decoupling for voltage reference
	VREF_MIC	O	Microphone bias voltage output
	LINER	I	Right channel line-in input
	MICR	I	Right channel microphone PGA positive input
	VOUTL	O	Left channel DAC driver amplifier output
	VOUTR	O	Right channel DAC driver amplifier output
	AOMS	I	Headphone virtual ground feedback
	AOM	O	Headphone virtual ground output
	HPDET		Headphone jack detection

Interface	Pin Name	Direction	Description
HDMI	EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current
	TX3N	O	TMDS negative clock line
	TX3P	O	TMDS positive clock line
	TX0N	O	TMDS channel 0 negative data line
	TX0P	O	TMDS channel 0 positive data line
	TX1N	O	TMDS channel 1 negative data line
	TX1P	O	TMDS channel 1 positive data line
	TX2N	O	TMDS channel 2 negative data line
	TX2P	O	TMDS channel 2 positive data line

Interface	Pin Name	Direction	Description
SAR-ADC	SARADC_AIN[i] (i=0~2)	N/A	SAR-ADC input signal for 3 channel

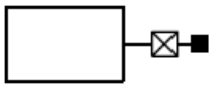
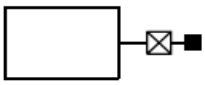
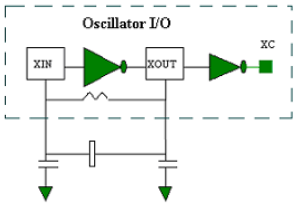
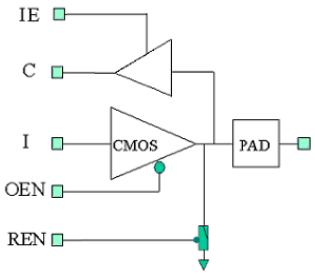
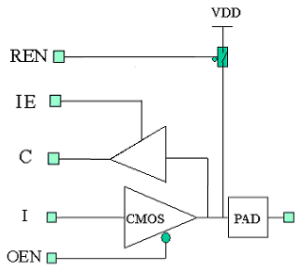
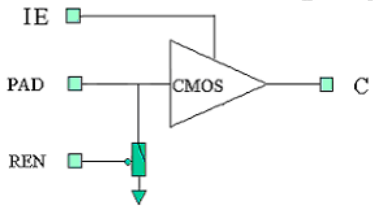
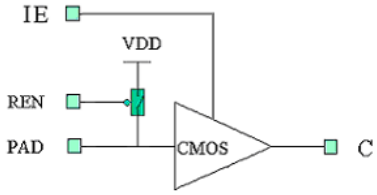
Interface	Pin Name	Direction	Description
eFuse	EFUSE_VP	N/A	eFuse program and sense power

1.3.4 RK3128 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 1-4 RK3128 IO Type List

Type	Diagram	Description	Pin Name

A		Analog IO Cell with IO voltage	EFUSE_VP
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with internal register	XIN24M/XOUT24M
D		CMOS 3-state output pad with controllable input and controllable pulldown	Part of digital GPIO (PBCDxRNC)
E		CMOS 3-state output pad with controllable input and controllable pullup	Part of digital GPIO (PBCUxRNC)
F		controllable input pad with controllable pulldown	Part of digital GPIO (PICDRNC)
G		controllable input pad with controllable pullup	Part of digital GPIO (PICURNC)

1.4 Package information

The package for RK3128 is TFBGA316(RK3128)
(body: 14mm x 14mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

1.4.1 TFBGA316 Dimension

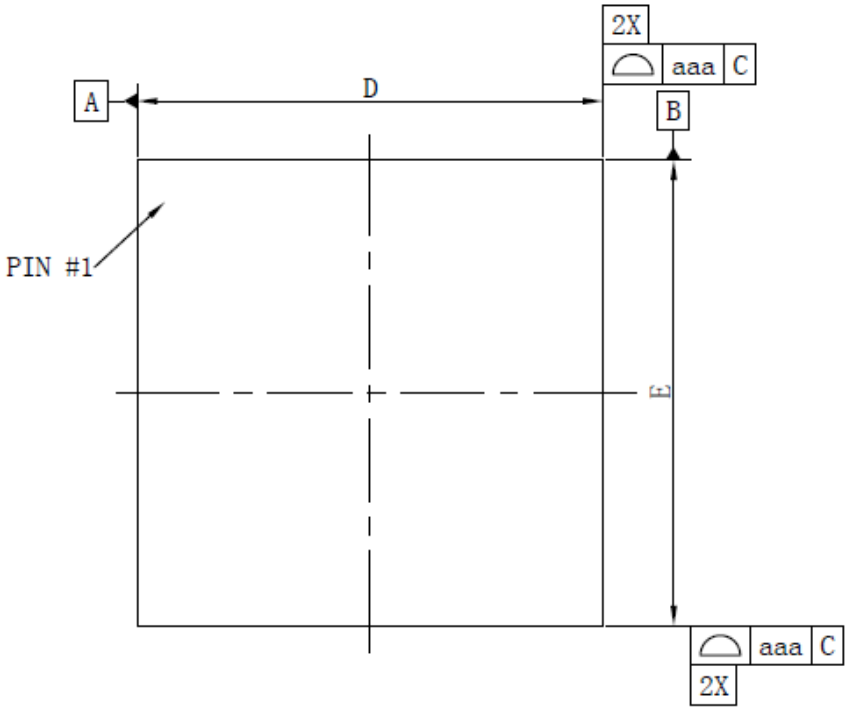


Fig.1-2RK3128 TFBGA316 Package Top View

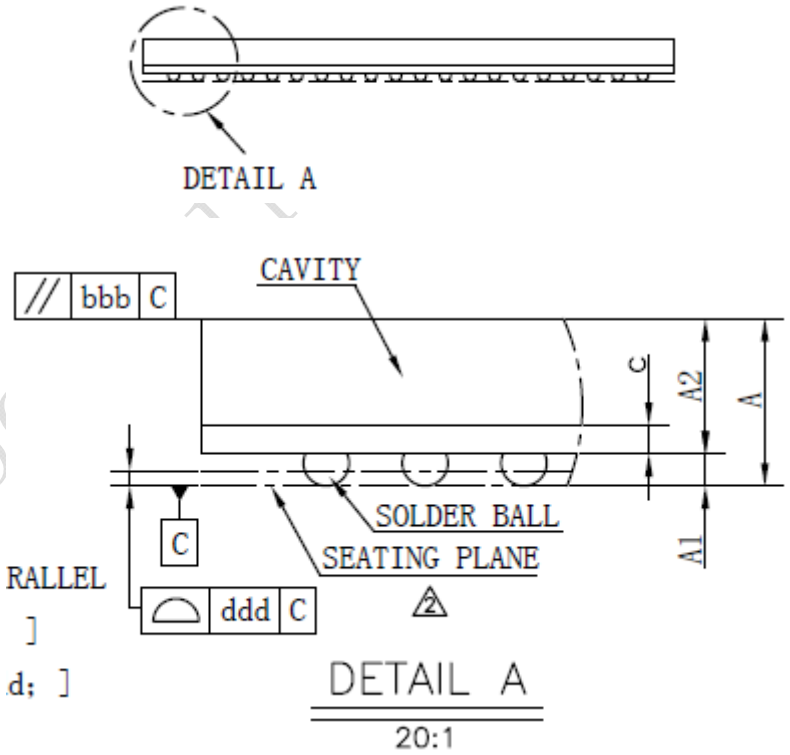


Fig.1-3RK3128 TFBGA316 Package Side View

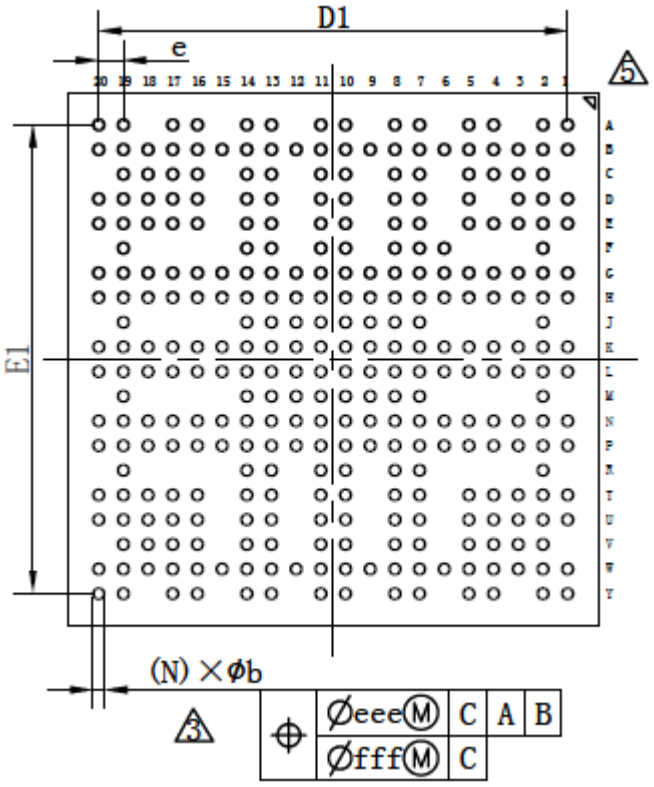


Fig.1-4RK3128 TFBGA316 Package Bottom View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.200	—	—	0.047
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.840	0.890	0.940	0.033	0.035	0.037
c	0.150	0.190	0.230	0.006	0.007	0.009
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	—	12.350	—	—	0.486	—
E1	—	12.350	—	—	0.486	—
e	—	0.650	—	—	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
N	316			316		
MD/ME	20/20			20/20		

Fig.1-5RK3128 TFBGA316 Package Dimension

1.4.2 TFBGA316 Ball Map

316	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	DDR_CSN0	DDR_A4	NP	DDR_A1	DDR_A15	NP	DDR_DQ3	DDR_DQS0	NP	DDR_DQ16	DDR_DQS2	NP	DDR_DQ23	DDR_DQ0	NP	CODEC_AOMS	CODEC_VCM	NP	GPIO0_D1/UART2_CTSN	GPIO0_D6/SDMMC1_PWR	A
B	DDR_CLK	DDR_ODT0	DDR_CKE	DDR_A12	DDR_A14	DDR_CSN1	DDR_DM0	DDR_DQS0_N	DDR_DQ18	DDR_DQ4	DDR_DQS2_N	DDR_DQ21	DDR_DQ6	VSS22	CODEC_AOR	CODEC_AOM	CODEC_AOL	CODEC_MICBIAS	GPIO1_B4/SPI_CSN1	GPIO0_A6/HDMI_SCL/I2C3_SCL	B
C	NP	DDR_CLK_N	VSS54	DDR_A10	DDR_A11	NP	VSS1	DDR_DQ7	NP	VSS2	DDR_DQ17	NP	VSS7	CODEC_HPDET	NP	CODEC_AIL	GPIO0_D0/UART2_RTSN/PMIC_SLEEP	GPIO3_C6	GPIO0_C4/HDMI_CEC	NP	C
D	DDR_A0	DDR_A3	DDR_BA2	NP	DDR_WEN	NP	DDR_BA0	DDR_A8	NP	DDR_DQ5	DDR_DM2	NP	CODEC_AVDD	CODEC_AVSS	NP	CODEC_AIR	GPIO0_A3/I2C1_SDA/SDMMC1_CMD	GPIO1_B7/SDMMC0_CMD	GPIO3_C4	GPIO0_A0/I2C0_SCL	D
E	DDR_A9	DDR_A2	DDR_RASN	DDR_A7	DDR_A5	NP	DDR_CASN	DDR_BA1	NP	、	DDR_DQ19	NP	GPIO0_B7/HDMI_HPD	CODEC_MICL	NP	CODEC_MICR	GPIO0_A1/I2C0_SDA	GPIO1_A1/I2S_SCLK/SDMMC1_D0/PMIC_S	GPIO1_A2/I2S_LRCK_RX/SDMMC1_D1	GPIO1_A0/I2S_MCLK/SDMMC1_CLKO/XIN_	E
F	NP	DDR_DQ10	NP	NP	NP	DDR_RESETN	DDR_A6	DDR_DQ1	NP	DDR_DQ22	DDR_DQ2	NP	GPIO3_C5	GPIO0_A7/HDMI_SDA/I2C3_SDA	NP	NP	NP	NP	GPIO0_A2/I2C1_SCL	NP	F
G	DDR_A13	DDR_ODT1	VSS3	DDR_DQ26	DDR_DQ9	DDR_DQ8	CVDD1	DDR_VDD5	DDR_VDD6	CVDD6	DDR_VDD7	DDR_VDD8	VSS6	VCCIO4	GPIO1_A3/I2S_LRCK_TX	GPIO1_A4/I2S_SDO/SDMMC1_D2	GPIO1_A5/I2S_SDI/SDMMC1_D3	GPIO1_B3/UART1_RTSN/SPI_CSN0	GPIO1_B0/UART1_CTSN/SPI_CLK	GPIO3_C7	G
H	DDR_DQS1	DDR_DQS1_N	DDR_DQ12	DDR_DM1	DDR_DQ28	DDR_DQ11	DDR_VDD4	VSS15	VSS16	VSS17	VSS18	VSS19	VSS20	CVDD5	TEST	GPIO0_B4/I2S_LRCK_TX	GPIO0_B0/I2S_MCLK	GPIO1_B1/UART1_TX/SPI_TXD	GPIO1_B2/UART1_RX/SPI_RXD	GPIO1_C0/SDMMC0_CLKO	H

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
J	NP	DDR_DQ13	NP	NP	NP	NP	DDR_VDD3	VSS23	VSS24	VSS25	VSS26	VSS27	VSS28	CVDD4	NP	NP	NP	NP	GPIO0_B3/I2S_LRCK_RX/SPI_TXD	NP	J
K	DDR_DQ15	DDR_DQ14	VSS4	DDR_DQ24	DDR_DQ27	DDR_DQ29	CVDD2	VSS21	VSS29	VSS30	VSS46	VSS31	VSS32	VCCIO3	GPIO1_C3/SDMMC0_D1/UART2_RX	GPIO1_C4/SDMMC0_D2/JTAG_TCK	GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_C	GPIO3_D7/CIF_PDN0/TEST_CLKO	GPIO0_B6/I2S_SDI/SPI_CSN0	GPIO0_B1/I2S_SCLK/SPI_CLK	K
L	DDR_DQS3	DDR_DQS3_N	DDR_DM3	DDR_DQ25	DDR_DQ30	DDR_DQ31	DDR_VDD2	VSS33	VSS34	VSS35	VSS36	VSS37	VSS38	VSS39	GPIO2_A3/FLASH_RDN/SFC_CSN1	GPIO2_A6/FLASH_CS0	GPIO0_C7/FLASH_CS1	GPIO1_C2/SDMMC0_D0/UART2_TX	GPIO1_A7/SDMMC0_WP	GPIO0_B5/I2S_SDO/SPI_RXD	L
M	NP	VSS5	NP	NP	NP	NP	DDR_VDD1	VSS40	VSS41	VSS42	VSS43	VSS44	VSS45	AVDD5	NP	NP	NP	NP	GPIO1_C5/SDMMC0_D3/JTAG_TMS	NP	M
N	XOUT24M	XIN24M	A/GPLL_VDD11	C/DPLL_VDD11	PLL_VCCIO	VCCIO1	VSS47	VSS48	VSS49	VSS50	VSS51	VSS52	VSS53	AVDD4	GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0	GPIO2_A0/FLASH_ALE/SPI_CLK	GPIO2_A1/FLASH_CLE	GPIO1_B6/SDMMC0_PWR	GPIO2_A7/FLASH_DQS/EMMC_CLKO	NPOR	N
P	GPIO2_C2/LCDC_D16/EBC_GDSP/GMAC_T	GPIO2_C3/LCDC_D17/EBC_GDPWR0/GMA	GPIO2_C5/LCDC_D19/EBC_SDSHR/I2C2_S	GPIO2_C7/LCDC_D21/EBC_BORDER1/GPS	GPIO2_C6/LCDC_D20/EBC_BORDER0/GPS	GPIO2_D0/LCDC_D22/EBC_GDPWR1/GPS_	VSS13	VSS8	SAR_AVDD33	CVDD3	ADCIN0	AVDD1	AVDD2	AVDD3	GPIO0_C1/CARD_IO/UART0_RTSN	GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0	GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1	GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD	GPIO1_C7/FLASH_CS3/EMMC_RST	GPIO2_A2/FLASH_WRN/SFC_CSN0	P
R	NP	GPIO2_C1/LCDC_D15/EBC_GDOE/GMAC_R	NP	NP	NP	NP	LVDS/MIPI_VCC1	LVDS/MIPI_VDD11	NP	EFUSE	USB0_ID	NP	CIF_D5/TS_D5	CIF_D6/TS_D6	NP	NP	NP	NP	GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD	NP	R
T	GPIO2_B7/LCDC_D13/EBC_SDCE5/GMAC_	GPIO2_D1/LCDC_D23/EBC_GDPWR2/GMA	GPIO2_C0/LCDC_D14/EBC_VCOM/GMAC_	GPIO2_C4/LCDC_D18/EBC_GDRL/I2C2_SD	GPIO2_B1/LCDC_HSYNC/EBC_SDLE/GMA	NP	VDAC_AVDD	VDAC_AGND	NP	USB_AVDD33	USB_DVDD11	NP	CIF_D4/TS_D4	VCCIO2	NP	CIF_D7/TS_D7	GPIO0_D3/PWM1	GPIO2_D2/CARD_RST/UART0_TX	GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2	GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3	T
U	GPIO2_B3/LCDC_DEN/EBC_GDCLK/GMAC	GPIO2_B5/LCDC_D11/EBC_SDCE3/GMAC_	GPIO2_B4/LCDC_D10/EBC_SDCE2/GMAC_	GPIO2_B6/LCDC_D12/EBC_SDCE4/GMAC_	GPIO2_B0/LCDC_CLK/EBC_SDCLK/GMAC_	NP	VDAC_IOUTN	VDAC_IREF	NP	ADCIN1	USB0_VBUS	NP	CIF_VSYNC/TS_SYNC	GPIO3_C1/DRIVE_VBUS/PMIC_SLEEP	NP	CIF_CLKI/TS_VALID	CIF_D0/TS_D0	GPIO0_D2/PWM0	GPIO1_C6/FLASH_CS2/EMMC_CMD	GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1	U
V	NP	HDMI_AVDD33	VSS14	HDMI_DVDD1V1_1	GPIO2_B2/LCDC_VSYNC/EBC_SDOE/GMA	NP	VDAC_IOUTP	LVDS/MIPI_EXTR	NP	ADCIN2	USB_EXTR	NP	CIF_CLKO/TS_CLKO	GPIO0_D4/PWM2	NP	CIF_D3/TS_D3	CIF_D1/TS_D1	CIF_HREF/TS_FAIL	GPIO2_A5/FLASH_WP/EMMC_PWR	NP	V
W	HDMI_TX3N	HDMI_TX0N	HDMI_EXTR	HDMI_TX1N	HDMI_TX2N	VSS9	LCDC_D9/LVDS_CLKN/EBC_SDCE1/MIPI	LCDC_D6/LVDS_TX3P/EBC_SDDO6/MIPI	VSS10	LCDC_D5/LVDS_TX2N/EBC_SDDO5/MIPI	LCDC_D3/LVDS_TX1N/EBC_SDDO3/MIPI	VSS12	LCDC_D1/LVDS_TX0N/EBC_SDDO1/MIPI	USB1_DP	VSS11	USB0_DP	CIF_D2/TS_D2	GPIO3_D2/IR	GPIO1_C1/SDMMC0_DET	GPIO2_D5/CARD_DET/UART0_CTSN	W
Y	HDMI_TX3P	HDMI_TX0P	NP	HDMI_TX1P	HDMI_TX2P	NP	LCDC_D8/LVDS_CLKP/EBC_SDCE0/MIPI	LCDC_D7/LVDS_TX3N/EBC_SDDO7/MIPI	NP	LCDC_D4/LVDS_TX2P/EBC_SDDO4/MIPI	LCDC_D2/LVDS_TX1P/EBC_SDDO2/MIPI	NP	LCDC_D0/LVDS_TX0P/EBC_SDDO0/MIPI	USB1_DM	NP	USB0_DM	GPIO2_D3/CARD_CLK/UART0_RX	NP	GPIO3_D3/SPDIF	CIF_PDN1/GPIO3_B3	Y

Fig.1-6TFBGA316 Ball Map

1.5 Electrical Specification

1.5.1 Absolute Maximum Ratings

Table 1-5 RK3128 absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	AVDD,CVDD, USB_DVDD11,HDMI_DVDD1V1_1	TBD	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	VCCIO1,VCCIO2,VCCIO3,VCCIO4	3.6	V
DC supply voltage for DDR IO	DDR_VDD	1.95	V
DC supply voltage for Analog part of SAR-ADC	SAR_AVDD33	3.6	V
DC supply voltage for Analog part of PLL	PLL_VCCIO A/DPLL_DVDD11,C/GPLL_DVDD11	3.3 1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD33	3.63	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD33	3.63	V
DC supply voltage for Analog part of Acodec	CODEC_AVDD	3.63	V
Analog Input voltage for SAR-ADC		2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature		80	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

1.5.2 Recommended Operating Conditions

Table 1-6 RK3128 recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power	AVDD,CVDD, USB_DVDD11,HDMI_DVDD1V1_1	TBD	1.1	TBD	V
Digital GPIO Power(3.3V)	VCCIO1,VCCIO2, VCCIO3,VCCIO4	2.97	3.3	3.63	V
DDR IO (DDRIII mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (LVDDRIII mode) Power	DDR_VDD	1.28	1.35	1.45	V
PLL Analog Power	PLL_VCCIO	2.97	3.3	3.63	V
PLL Analog Power	A/DPLL_DVDD11 ,C/GPLL_DVDD1	0.99	1.1	1.21	V

	1				
SAR-ADC Analog Power	SAR_AVDD33	2.97	3.3	3.63	V
SAR-ADC external reference Power	VREF	0.2* SAR_AVDD33		0.9* SAR_AVDD33	
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	130.5	135	139.5	Ohm
Acodec Analog Power	CODEC_AVDD	2.97	3.3	3.63	V
HDMI Analog Power	HDMI_AVDD33	2.97	3.3	3.63	V
TV EncoderAnalog Power	ADDHV6	2.97	3.3	3.63	V
EFUSE programming voltage		N/A	2.5	N/A	V
PLL input clock frequency		N/A	24	N/A	MHz
Operating Temperature		-40	25	85	℃

1.5.3 DC Characteristics

Table 1-7 RK3128 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2	3.3	3.6	V
	Output Low Voltage	Vol	N/A	0	0.4	V
	Output High Voltage	Voh	2.4	3.3	N/A	V
	Threshold Point	Vt	1.21	1.42	1.64	V
	Schmitt trig Low to High threshold point	Vt+	1.36	1.6	1.86	V
	Schmitt trig High to Low threshold point	Vt-	0.93	1.09	1.3	V
	Pullup Resistor	Rpu	33	41	62	Kohm
	Pulldown Resistor	Rpd	33	42	68	Kohm
DDR IO @DDRIII mode	Input High Voltage	Vih_ddr	VREFi + 0.125 (i=0~2)	1.8	VDDIO_DDRi + 0.3 (i=0~6)	V
	Input Low Voltage	Vil_ddr	-0.3	0	VREFi - 0.125 (i=0~2)	V
	Output High Voltage	Voh_ddr	VDDIO_DDRi - 0.28 (i=0~6)	1.8	N/A	V
	Output Low	Vol_ddr	N/A	0	0.28	V

	Voltage					
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	120 60 40	150 75 50	180 90 60	Ohm
DDR IO @LPDDR mode	Input High Voltage	Vih_ddr	0.7*VDDIO_DDRi (i=0~6)	1.8	N/A	V
	Input Low Voltage	Vil_ddr	N/A	0	0.3*VDDIO_DDRi (i=0~6)	V
PLL	Input High Voltage	Vih_pll	0.8*DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	V
	Input Low Voltage	Vil_pll	0	0	0.2*DVDD_iPLL (i=A,D,CG)	V
HDMI	single-ended high level output voltage, VH(when sink <=165Mhz)	Voh	HDMI_AVDD33-10mv	N/A	HDMI_AVDD33+10mv	mV
	single-ended high level output voltage, VH(when sink > 165Mhz)	Voh	HDMI_AVDD33-200mv	N/A	HDMI_AVDD33+10mv	mV
	single-ended low level output voltage, VL (when sink <= 165Mhz)	Vol	HDMI_AVDD33 -600mv	N/A	HDMI_AVDD33-400mv	mV
	single-ended low level output voltage, VL (when sink > 165Mhz)	Vol	HDMI_AVDD33-700mv	N/A	HDMI_AVDD33-400mv	mv
	single-ended output swing voltage, Vswing	Vswing	400	N/A	600	mV
	single-ended standby (off) output voltage,	Voff	HDMI_AVDD33 -10mv	N/A	HDMI_AVDD33+10mv	mv
	single-ended standby (off) output	Ioff	-10	N/A	10	uA

	current					

1.5.4 Recommended Operating Frequency

Table 1-8 Recommended operating frequency for PLL and oscillator domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	1.1V , 25 ℃	XIN24M	24	24	24	MHz
	1.21V , -40 ℃		24	24	24	
	0.99V , 125 ℃		24	24	24	
DDR PLL	1.1V , 25 ℃	ddr_pll_clk	N/A	N/A	1050	MHz
	1.21V , -40 ℃		N/A	N/A	1176	
	0.99V , 125 ℃		N/A	N/A	950	
ARM PLL	1.1V , 25 ℃	arm_pll_clk	N/A	N/A	1086	MHz
	1.21V , -40 ℃		N/A	N/A	1176	
	0.99V , 125 ℃		N/A	N/A	850	
CODEC PLL	1.1V , 25 ℃	cocec_pll_clk	N/A	N/A	880	MHz
	1.21V , -40 ℃		N/A	N/A	1000	
	0.99V , 125 ℃		N/A	N/A	770	
GENERAL PLL	1.1V , 25 ℃	general_pll_clk	N/A	N/A	900	MHz
	1.21V , -40 ℃		N/A	N/A	940	
	0.99V , 125 ℃		N/A	N/A	780	

Table 1-9 Recommended operating frequency for CPU core

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
Cortex-A7	1.1V , 25 ℃	CORE_SRC_CLK	N/A	N/A	TBD	MHz
	1.21V , -40 ℃		N/A	N/A	TBD	
	0.99V , 125 ℃		N/A	N/A	790	
	1.1V , 25 ℃	aclk_core_pre	N/A	N/A	TBD	MHz
	1.21V , -40 ℃		N/A	N/A	TBD	
	0.99V , 125 ℃		N/A	N/A	400	

Table 1-10 Recommended operating frequency for PD_CPU domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
CPU AXI interconnect	1.1V , 25 ℃	CPU_ACLK	N/A	N/A	500	MHz
	1.21V , -40 ℃		N/A	N/A	650	
	0.99V , 125 ℃		N/A	N/A	300	
	1.1V , 25 ℃	CPU_HCLK	N/A	N/A	320	MHz
	1.21V , -40 ℃		N/A	N/A	470	
	0.99V , 125 ℃		N/A	N/A	180	
	1.1V , 25 ℃	CPU_PCLK	N/A	N/A	90	MHz
	1.21V , -40 ℃		N/A	N/A	90	
	0.99V , 125 ℃		N/A	N/A	80	

DMC	1.1V , 25 ℃	DDR_PHY1X_CLK	N/A	N/A	900	MHz
	1.21V , -40 ℃		N/A	N/A	760	
	0.99V , 125 ℃		N/A	N/A	400	

Table 1-11 Recommended operating frequency for PD_PERI domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
PERI AXI interconnect	1.1V , 25 ℃	PERI_ACLK	N/A	N/A	470	MHz
	1.21V , -40 ℃		N/A	N/A	600	
	0.99V , 125 ℃		N/A	N/A	300	
	1.1V , 25 ℃	PERI_HCLK	N/A	N/A	180	MHz
	1.21V , -40 ℃		N/A	N/A	200	
	0.99V , 125 ℃		N/A	N/A	150	
	1.1V , 25 ℃	PERI_PCLK	N/A	N/A	80	MHz
	1.21V , -40 ℃		N/A	N/A	88	
	0.99V , 125 ℃		N/A	N/A	75	
NANDC	1.1V , 25 ℃	FLASH_HCLK	N/A	N/A	190	MHz
	1.21V , -40 ℃		N/A	N/A	220	
	0.99V , 125 ℃		N/A	N/A	150	
USB OTG	1.1V , 25 ℃	UTMI_CLK_0/ UTMI_CLK_1	N/A	N/A	140	MHz
	1.21V , -40 ℃		N/A	N/A	200	
	0.99V , 125 ℃		N/A	N/A	76	
UART0/1/2	1.1V , 25 ℃	UART0_CLK/ UART1_CLK/ UART2_CLK	N/A	N/A	50	MHz
	1.21V , -40 ℃		N/A	N/A	50	
	0.99V , 125 ℃		N/A	N/A	50	
SDMMC/SDIO	1.1V , 25 ℃	MMC0_CLK/ SDIO_CLK	N/A	N/A	50	MHz
	1.21V , -40 ℃		N/A	N/A	50	
	0.99V , 125 ℃		N/A	N/A	50	
eMMC	1.1V , 25 ℃	eMMC_CLK	N/A	N/A	100	MHz
	1.21V , -40 ℃		N/A	N/A	100	
	0.99V , 125 ℃		N/A	N/A	100	
I2S	1.1V , 25 ℃	I2S_CLK	N/A	N/A	50	MHz
	1.21V , -40 ℃		N/A	N/A	50	
	0.99V , 125 ℃		N/A	N/A	50	
SPI0	1.1V , 25 ℃	SPI0_CLK	N/A	N/A	50	MHz
	1.21V , -40 ℃		N/A	N/A	50	
	0.99V , 125 ℃		N/A	N/A	50	
SAR-ADC	1.1V , 25 ℃	SARADC_CLK	N/A	N/A	12	MHz
	1.21V , -40 ℃		N/A	N/A	12	
	0.99V , 125 ℃		N/A	N/A	12	
Timer0/1	1.1V , 25 ℃	TIMER0_CLK/	N/A	N/A	24	MHz

	1.21V , -40 ℃	TIMER1_CLK	N/A	N/A	24	
	0.99V , 125 ℃		N/A	N/A	24	
	1.1V , 25 ℃	TIMER0_PCLK/ TIMER1_PCLK	N/A	N/A	140	MHz
	1.21V , -40 ℃		N/A	N/A	190	
	0.99V , 125 ℃		N/A	N/A	75	

Table 1-12 Recommended operating frequency for PD_VIO domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
Display AXI interconnection	1.1V , 25 ℃	DISP_ACLK	N/A	N/A	520	MHz
	1.21V , -40 ℃		N/A	N/A	700	
	0.99V , 125 ℃		N/A	N/A	300	
	1.1V , 25 ℃	DISP_HCLK	N/A	N/A	360	MHz
	1.21V , -40 ℃		N/A	N/A	500	
	0.99V , 125 ℃		N/A	N/A	200	
LCDC	1.1V , 25 ℃	LCDC_DCLK	N/A	N/A	200	MHz
	1.21V , -40 ℃		N/A	N/A	230	
	0.99V , 125 ℃		N/A	N/A	150	
	1.1V , 25 ℃	LCDC1_DCLK	N/A	N/A	200	MHz
	1.21V , -40 ℃		N/A	N/A	240	
	0.99V , 125 ℃		N/A	N/A	160	
CIF	1.1V , 25 ℃	IO_CIF_CLKIN	N/A	N/A	100	MHz
	1.21V , -40 ℃		N/A	N/A	100	
	0.99V , 125 ℃		N/A	N/A	100	

Table 1-13 Recommended operating frequency PD_GPU domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
GPU	1.1V , 25 ℃	GPU_ACLK	N/A	N/A	550	MHz
	1.21V , -40 ℃		N/A	N/A	720	
	0.99V , 125 ℃		N/A	N/A	300	

Table 1-14 Recommended operating frequency for PD_VIDEO domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
VIDEO	1.1V , 25 ℃	VEPU_ACLK	N/A	N/A	490	MHz
	1.21V , -40 ℃		N/A	N/A	650	
	0.99V , 125 ℃		N/A	N/A	300	
	1.1V , 25 ℃	hclk_vepu	N/A	N/A	200	MHz
	1.21V , -40 ℃		N/A	N/A	225	
	0.99V , 125 ℃		N/A	N/A	150	
	1.1V , 25 ℃	VDPU_ACLK	N/A	N/A	420	MHz
	1.21V , -40 ℃		N/A	N/A	610	
	0.99V , 125 ℃		N/A	N/A	280	
	1.1V , 25 ℃	hclk_vdpu	N/A	N/A	200	MHz

	1.21V , -40 ℃		N/A	N/A	220	
	0.99V , 125 ℃		N/A	N/A	150	

1.5.5 Electrical Characteristics for General IO

Table 1-15 RK3128 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Il	Vin = 3.3V or 0V	-1	N/A	1	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	-1	N/A	1	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 3.3V, pulldown enabled	TBD	TBD	TBD	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	TBD	TBD	TBD	uA

1.5.6 Electrical Characteristics for PLL

Table 1-16 RK3128 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency	Fin	Fin = FREF @3.3V/1.1V①	1/10	24	800	MHz
	Comparison frequency	Fref	FREF = Fin/REFDIV @3.3V/1.1V	1	N/A	40	MHz
	VCO operating range	Fvco	Fvco = Fref * FBDIV① @3.3V/1.1V	400	N/A	1600	MHz
	Output clock frequency	Fout	Fout = Fvco/POSTDIV① @3.3V/1.1V	1	N/A	1600	MHz
	Lock time②	Tlt	@ 3.3V/1.1V, FREF=24M,REFDIV=1	N/A	41.7	62.5	us
	VDDHV Power consumption ③ (normal mode)	N/A	Fvco = 1000MHz, @3.3V, 25 ℃	N/A	1	1.2	mA
	VDD Power consumption (normal mode)	N/A	@3.3V/1.1V, 25 ℃	N/A	3	4	uW/MHz
	Power consumption (bypass mode)	N/A	BYPASS=HIGH , PD= LOW , Fin = 24MHz, Fout = 24MHz, @3.3V/1.1V, 25 ℃	N/A	N/A	N/A	uW
	Power consumption (power-down mode)	N/A	PD=HIGH, @27 ℃	N/A	10	N/A	uA

Notes :

①:REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value

②Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks

in max.
⑧Current scale as (Fvco/1GHz)[1.5]

1.5.7 Electrical Characteristics for SAR-ADC

Table 1-17 RK3128 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Conversion speed	Fs		N/A	N/A	N/A	MSPS
Differential Non Linearity	DNL		N/A	N/A	N/A	LSB
Integral Nn Linearity	INL		N/A	N/A	N/A	LSB
Gain Error	Egain		N/A	N/A	N/A	%FS
Offset Error	Eoffset		N/A	N/A	N/A	%FS
Input Range	CH[2:0]	3-channel single-ended input	0.01* SAR_AVDD33	N/A	0.99* SAR_AVDD33	V
Input Resistance	RIN		N/A	N/A	N/A	Kom
Input Capacitance	CIN		N/A	1	N/A	pF
Sampling Clock			N/A	200	N/A	KHz
Main Clock Frequency	CLK		N/A	2.2	N/A	MHz
Data Latency			N/A	11	N/A	Clock Cycle
SNR plus Distortion(Up to 5th harmonic)	SINAD	Fin=10K Fin=99K	N/A	61.49 60.58	N/A	dB
Spurious-Free Dynamic Range	SFDR	Fin=10K Fin=99K	N/A	66.29 67.14	N/A	dB
Second-Harmonic Distortion	2HD	Fin=10K Fin=99K	N/A	-72.64 -69.94	N/A	dB
Third-Harmonic Distortion	3HD	Fin=10K Fin=99K	N/A	-74.79 -68.85	N/A	dB
Effective Number of Bits	ENOB	Fin=10K Fin=99K	N/A	9.92 9.77	N/A	Bits
Positive Reference	VREF		0.2* SARADC_AVDD33		0.9* SARADC_AVDD33	V
Analog Supply Current(SARADC_VDDA)			N/A	N/A	200	uA
Digital Supply Current			N/A	N/A	50	uA
Reference Supply Current			N/A	N/A	50	uA
Power Down Current			N/A	N/A	N/A	uA
Power up time			N/A	N/A	N/A	1/Fs

1.5.8 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 1-18 RK3128 Electrical Characteristics for USB OTG/Host2.0 Interface

1.5.9 Electrical Characteristics for HDMI

Parameters		Test condition	Min	Typ	Max	Units
HS transmit,(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33	USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	N/A	N/A	0.1	mA
	Current From USB_DVDD11		N/A	N/A	20	mA
Classic mode active(quiescent supply current;	Current From USB_AVDD33		N/A	N/A	0.5	mA
	Current From		N/A	N/A	0.5	mA

Vin=0 or 1)	USB_DVDD11					
HS mode(CL=10pF) Active supply current	Current From USB_AVDD33		N/A	0.1	N/A	mA
	Current From USB_DVDD11		N/A	2.22	N/A	mA
FS transmit,(CL=50pF) Active supply current	Current From USB_AVDD33		N/A	10	30	mA
	Current From USB_DVDD11		N/A	5	10	mA
LS transmit(CL=50 to 350pF) Active supply current	Current From USB_AVDD33		N/A	2	25	mA
	Current From USB_DVDD11		N/A	2	5	mA
Suspend mode	Current From USB_AVDD33		N/A	N/A	50	uA
	Current From USB_DVDD11		N/A	N/A	5	uA

Table 1-19 RK3128 Electrical Characteristics for HDMI

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
	rise time/fall time(20%-80%)	Tfall/Trise		75	N/A	0.4Tbit	ps
	overshoot, max			15% of full differential amplitude(Vswing*2)			ps
	undershoot, max			25% of full differential amplitude(Vswing*2)			ps
	Intra-pair skew at transmitter connector, max			N/A	N/A	0.15 Tbit	ps
	inter-pair skew at transmitter connector, max			N/A	N/A	0.2 Tpixel	ps
	TMDS Differential clock jitter, max			N/A	N/A	0.25 Tbit	ps
	clock duty cycle			40%	N/A	60%	

1.5.10 Electrical Characteristics for DDR IO

Table 1-20 RK3128 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	DDR IO power standby current, ODT OFF		@ 1.5V , 125℃	N/A	N/A	N/A	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	N/A	N/A	N/A	uA
DDR IO @LVDDR3 mode	Input leakage current		@ 1.35V , 125℃	N/A	N/A	N/A	uA
	DDR IO power quiescent current		@ 1.35V , 125℃	N/A	N/A	N/A	uA

1.5.11 Electrical Characteristics for eFuse

Table 1-21 RK3128 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	read current	Iactive	STROBE high	N/A	2.53	N/A	mA
standby mode	standby current	Istandby		N/A	0.4	N/A	uA
power-down mode	power-down current	Ipd_vdd		N/A	N/A	N/A	uA
Peak program current	Peak program current	Iprog		N/A	20.8	N/A	mA

1.5.12 Electrical Characteristics for TV Encoder

Table 1-22 RK3128 Electrical Characteristics for TV Encoder

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Bandgap Voltage	Vbg		N/A	1.21	N/A	V
Reference Resistor		E96 series	N/A	1130	N/A	ohm
Reference Current			N/A	1.07	N/A	mA
Output Full Scale Current		Programmable through dacXgc5..0 word (external load of 37.5Ohm) Refer to Operating Modes for details	N/A	N/A	34	mA
Resistive Load			N/A	37.5	N/A	Ohm
Offset Error			N/A	+/-1	N/A	%FS
Gain Error(DAC to DAC matching)			N/A	+/-2	N/A	%FS
Absolute Gain Error			N/A	+/-4	N/A	%FS
DNL		Ifs=34mA	N/A	+/-0.5	N/A	LSB
INL		Ifs=34mA	N/A	+/-1.0	N/A	LSB
Update Rate			1	N/A	300	MHz
Startup Time		From Complete shut-down to normal operation	N/A	3	4	Us
Cable sensing Cycle time		Details on Cable Sensing Cycle Timing Diagram	N/A	4.5	N/A	Clk cycles
SFDR	SFDR	Fout=5MHz, Ifs=34mA, RL=37.5ohm, Fs=300MHz	N/A	58	N/A	dBc
		Fout=1MHz, Ifs=34mA,	N/A	61	N/A	dBc

		RL=37.5ohm, Fs=300MHz				
SINAD	SINAD	Fout=5MHz, Ifs=34mA, RL=37.5ohm, Fs=300MHz	N/A	54	N/A	dBc
		Fout=1MHz, Ifs=34mA, RL=37.5ohm, Fs=300MHz	N/A	57	N/A	dBc
High Voltage Analog Current(avddhv6.0)		Ifs=34mA	N/A	51	N/A	mA
Digital Current(dvdd)		Fs=300MHz	N/A	0.7	N/A	mA
Power down current		High Voltage Analog supply and digital supply	N/A	60	N/A	uA

1.6 Hardware Guideline

1.6.1 Reference design for RK3128 oscillator PCB connection

RK3128 only use one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram ,Rf is used to bias the inverter in the high gain region. The recommend value is 1Mohm.
Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Rd of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.
C1 and C2 are deciding regard to the crystal or resonator CL specification.
the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model .

In RK3128, the crystal oscillator I/O cells have embedded internal resistor, so we need not add feedback resistor (Rf) as above description.

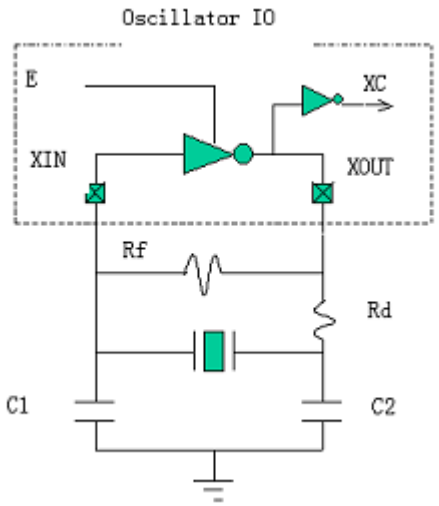


Fig.1-7 External Reference Circuit for 24MHzOscillators

1.6.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK3128.

For optimal jitter performance it is suggested to place external decoupling capacitorson the boardbetween VDDHV-VSS(PLL_VSS1) and
VDDPOST-VSS(PLL_VSS2) . VDDREF is typically connected to the global chipsupply and does not require dedicated decoupling.
It is recommended to use at least one large capacitor (e.g. 4.7uF) capacitor for each separate supply.Additionally, a 100nF and 10nF capacitor may be placed in parallel since the lead inductance of the4.7uF capacitor may be large.
Capacitors with minimal lead inductance should be selected. Ceramic type capacitors work well. Thecapacitors should be placed as close to the package pins as possible. No series impedance shouldbe added anywhere on the board, and impedance to the voltage source should be minimized.

1.6.3 Reference design for USB OTG/Host2.0 connection

In RK3128 there are USB OTG and USB Host2.0 interface, and they share a common PHY.

- Decouple Capacitance

We should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 1-9. Place these components as closely as possible to the power pins.

- Differential Lines

The differential lines should be routed together, minimizing the number of vias through which the signal lines are routed. Layout the differential pairs with controlled impedance of 100 ohm differential.

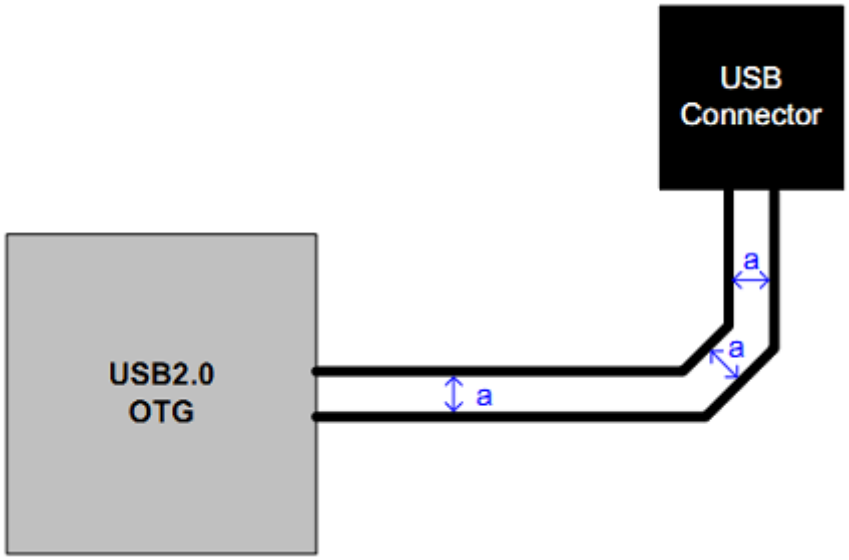


Fig.1-8RK3128 USB OTG/Host2.0 differential lines requirement.

If high-speed signals are routed on the Top layer, best results will be obtained if the Layer 2 is a Ground plane. Furthermore, there must have only one ground plane under high-speed signals in order to avoid the high-speed signals to cross another ground plane.

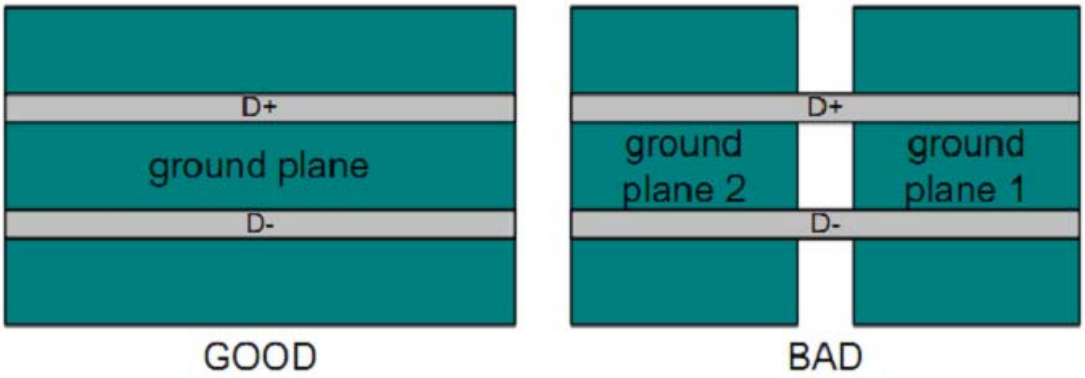


Fig.1-9RK3128 USB OTG/Host2.0 ground plane guide.

- Component Placement

  It is very important to not create stubs on the high-speed lines, to avoid that, the placement of component should be the closed as possible from D+ and D- lines, like shown in the following figure.

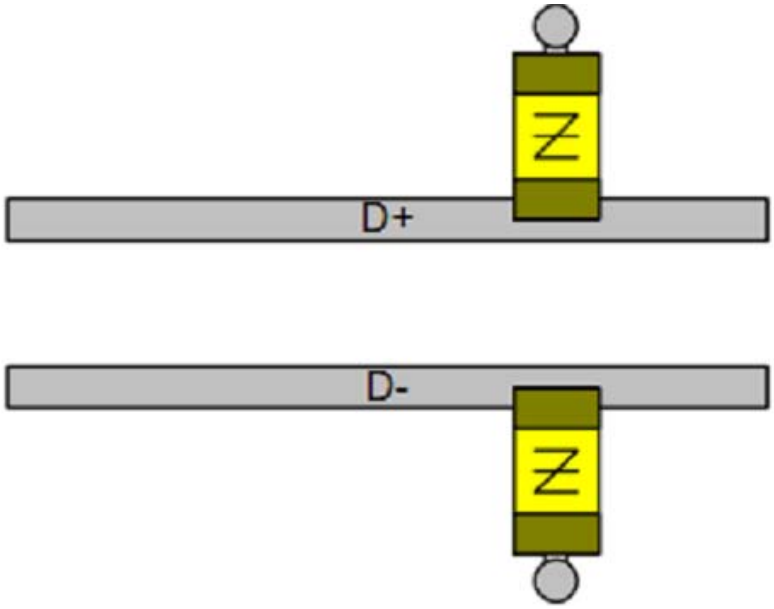


Fig.1-10RK3128 USB OTG/Host2.0 component placement.

1.6.4 Reference design for HDMI Tx PHY connection

In RK3128, the following diagram shows external PCB reference design for HDMI Tx PHY.It mainly introduces how to connect the TMDS channel, DDC channel, CEC channel and HPD signal of RK3128 HDMI Transmitter to the HDMI port type A.

- TMDS channel

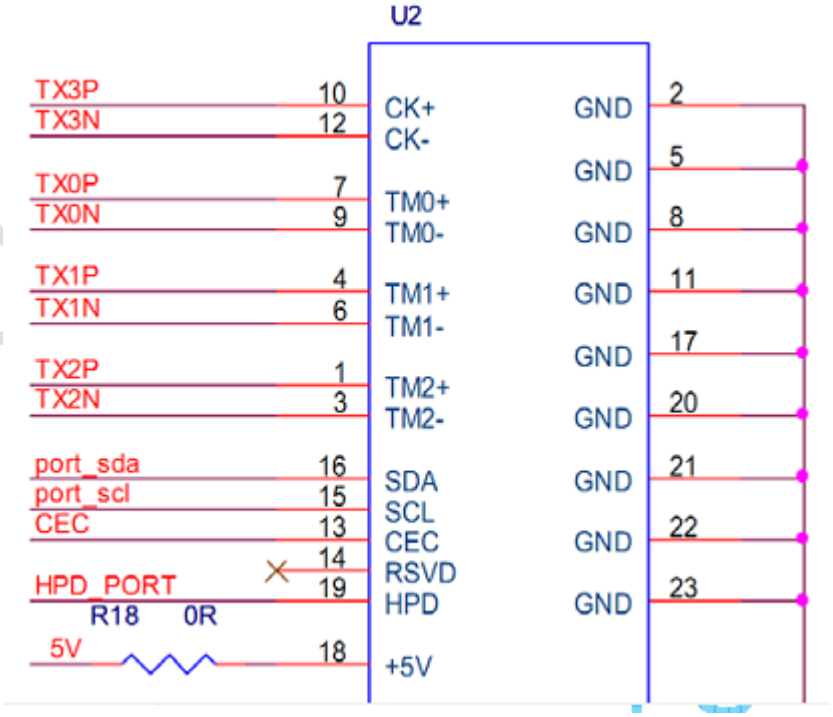


Fig.1-11RK3128 HDMI interface reference connection

- DDC channel

RK3128 can accept DDC_sda/DDC_scl 5V voltage input, it's no need to add additional Transmitter to transfer the DDC_sda/DDC_scl from 5V to 3.3V outside the chip.

- CEC channel

  RK3128 can accept CEC 5V voltage input, it's no need to add additional Transmitter to transfer the CEC from 5V to 3.3V outside the chip.

- HPD

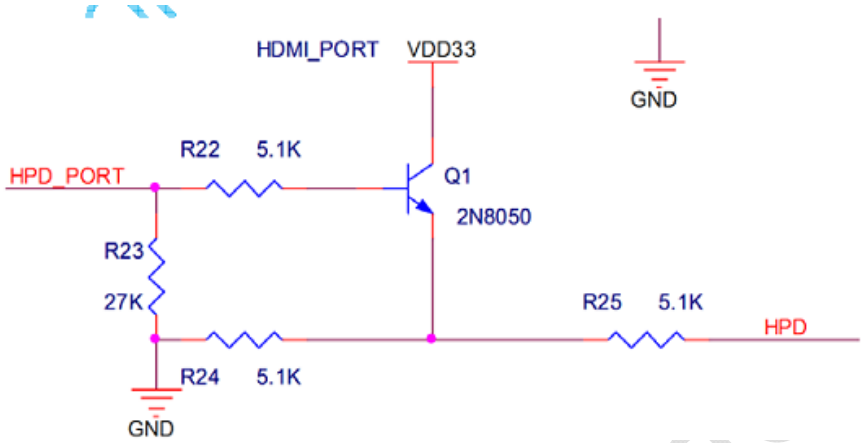


Fig.1-12RK3128 HDMI CEC interface reference connection

- ESD

  If ESD suppression devices or common mode chokes are used, place them near the HDMI connector.

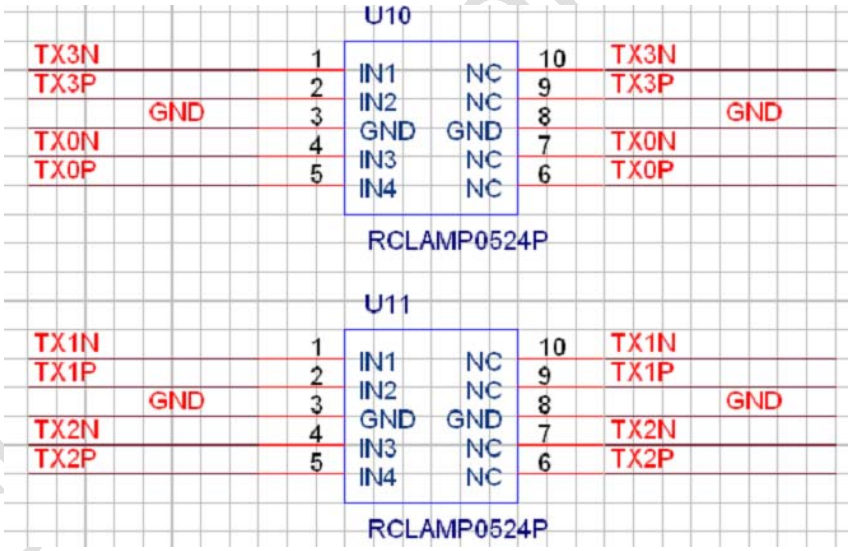


Fig.1-13RK3128 HDMI ESD interface reference connection

1.6.5 Reference design for Audio Codec connection

In RK3128, the following diagram shows external PCB reference design for Audio Codec.

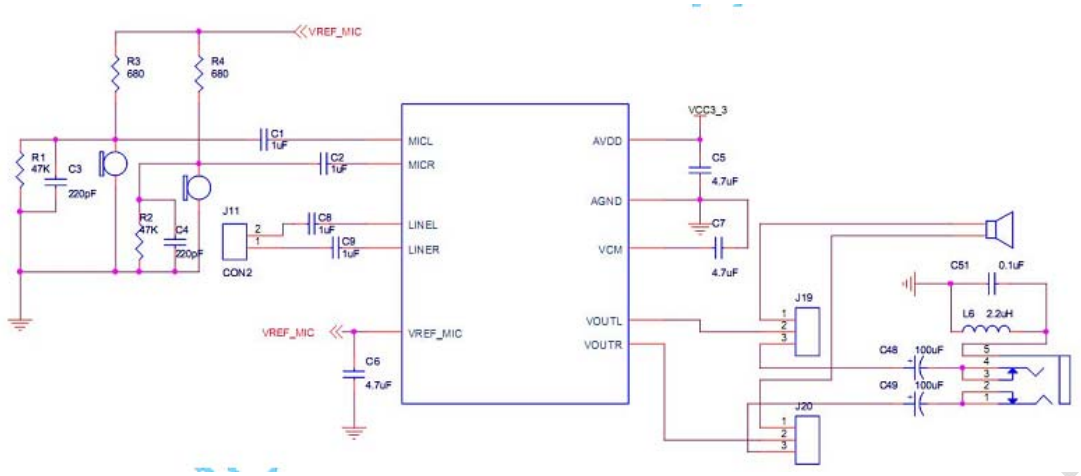


Fig.1-14RK3128 Audio Codec interface reference connection

As above diagram shows, the MICL and MICR are each connected with a MIC through a 1uf CAP, the LINEL and LINER have the same function as the MICL and MICR. The R1 and C3 are formed a filter for the MIC, and the R2, C4 have same function. The VREF_MIC is used for bias the MIC through a resistor. The resistor value should be changed according the MIC. The AVDD should be supplied by 3.3V. The CAP connected with AVDD should be placed as close as possible

The VCM is connected with GND through a 4.7Uf CAP. The CAP should be placed as close as possible. The VOUTL and VOUTR could be connected with a speaker or an earphone. When connecting with a speaker, they could connect it directly. When connecting with an earphone, they should connect it through a 100uF CAP. The J19 and J20 are dip-switches, and you could select a speaker or an earphone as the output.

1.6.6 RK3128 Power on reset descriptions

NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstndeassert, andthe PLL max lock time is 1500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

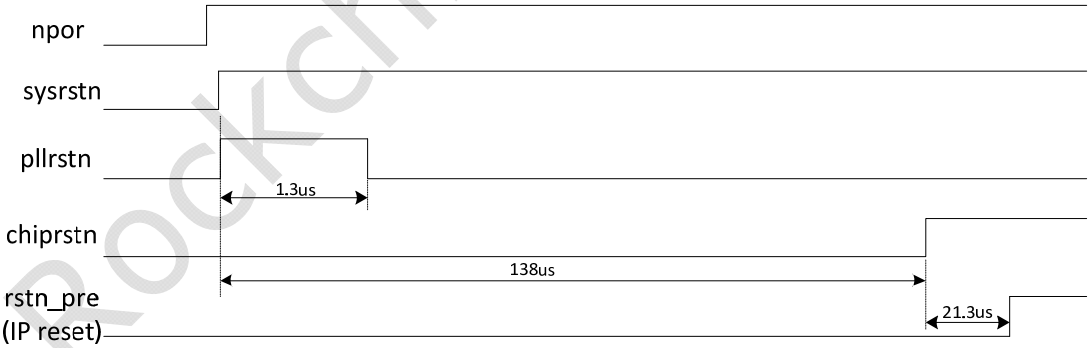


Fig.1-15 RK3128 reset signals sequence