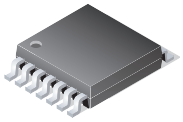
DirectPath™, 2-VRMS Audio Line Driver With Adjustable Gain

Check for Samples: DRV632



FEATURES

- **Stereo DirectPath™ Audio Line Driver**
  - **2 Vrms Into 10 kΩ With 3.3-V Supply**
- **Low THD+N < 0.01% at 2 Vrms Into 10 kΩ**
- **High SNR, >90 dB**
- **600-Ω Output Load Compliant**
- **Differential Input and Single-Ended Output**
- **Adjustable Gain by External Gain-Setting Resistors**
- **Low DC Offset, <1 mV**
- **Ground-Referenced Outputs Eliminate DC-Blocking Capacitors**
  - **Reduce Board Area**
  - **Reduce Component Cost**
  - **Improve THD+N Performance**
  - **No Degradation of Low-Frequency Response Due to Output Capacitors**
- **Short-Circuit Protection**
- **Click- and Pop-Reduction Circuitry**
- **External Undervoltage Mute**
- **Active Mute Control for Pop-Free Audio On/Off Control**
- **Space-Saving TSSOP Package**

APPLICATIONS

- **Set-Top Boxes**
- **Blu-ray Disc™, DVD Players**
- **LCD and PDP TV**
- **Mini/Micro Combo Systems**
- **Sound Cards**
- **Laptops**

DESCRIPTION

The DRV632 is a 2-V_{RMS} pop-free stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single-supply electronics where size and cost are critical design parameters.

Designed using TI's patented DirectPath™ technology, The DRV632 is capable of driving 2 V_{RMS} into a 10-kΩ load with 3.3-V supply voltage. The device has differential inputs and uses external gain-setting resistors to support a gain range of ±1 V/V to ±10 V/V, and gain can be configured individually for each channel. Line outputs have ±8-kV IEC ESD protection, requiring just a simple resistor-capacitor ESD protection circuit. The DRV632 has built-in active-mute control for pop-free audio on/off control. The DRV632 has an external undervoltage detector that mutes the output when the power supply is removed, ensuring a pop-free shutdown.

Using the DRV632 in audio products can reduce component count considerably compared to traditional methods of generating a 2-V_{RMS} output. The DRV632 does not require a power supply greater than 3.3 V to generate its 5.6-V_{pp} output, nor does it require a split-rail power supply. The DRV632 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased 2-V_{RMS} output.

The DRV632 is available in a 14-pin TSSOP.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C to 85°C	DRV632PW	14-Pin

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range

		VALUE	UNIT
	Supply voltage, VDD to GND	–0.3 to 4	V
V_I	Input voltage	V_{SS} – 0.3 to VDD + 0.3	V
R_L	Minimum load impedance – line outputs – OUTL, OUTR	600	Ω
	$\overline{\text{Mute}}$ to GND, UVP to GND	–0.3 to VDD + 0.3	V
T_J	Maximum operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–40 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV632 PW 14 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	130	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	49	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	63	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	62	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3	3.3	3.6	V
R_L	Load impedance		0.6	10		kΩ
V_{IL}	Low-level input voltage	$\overline{\text{Mute}}$		40		% of VDD
V_{IH}	High-level input voltage	$\overline{\text{Mute}}$		60		% of VDD
T_A	Operating free-air temperature		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage	VDD = 3.3 V		0.5	1	mV
PSRR	Power-supply rejection ratio			80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
V_{UVP_EX}	External UVP detect voltage			1.25		V
$V_{UVP\_EX\_HYSTERESIS}$	External UVP detect hysteresis current			5		µA
f_{CP}	Charge pump switching frequency		200	300	400	kHz
$\lvert I_{IH}\rvert$	High-level input current, $\overline{\text{Mute}}$	VDD = 3.3 V, V_{IH} = VDD			1	µA
$\lvert I_{IL}\rvert$	Low-level input current, $\overline{\text{Mute}}$	VDD = 3.3 V, V_{IL} = 0 V			1	µA
I_{DD}	Supply current	VDD = 3.3 V, no load, $\overline{\text{Mute}}$ = VDD	5	14	25	mA
		VDD = 3.3 V, no load, $\overline{\text{Mute}}$ = GND, disabled		14		

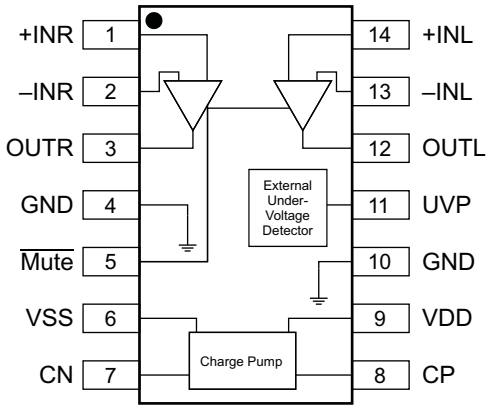
OPERATING CHARACTERISTICS

VDD = 3.3 V, R_{DL} = 10 kΩ, R_{FB} = 30 kΩ, R_{IN} = 15 kΩ, T_A = 25°C, Charge pump: C_P = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, outputs in phase	THD+N = 1%, VDD = 3.3 V, f = 1 kHz, R_L = 10 kΩ	2	2.4		V_{rms}
THD+N	Total harmonic distortion plus noise	V_O = 2 V_{RMS}, f = 1 kHz		0.002%		
SNR	Signal-to-noise ratio(1)	A-weighted	90	105		dB
DNR	Dynamic range	A-weighted	90	105		dB
V_N	Noise voltage	A-weighted		11		µV
Z_O	Output Impedance when muted	$\overline{\text{Mute}}$ = GND		110		mΩ
	Input-to-output attenuation when muted	$\overline{\text{Mute}}$ = GND		80		dB
	Crosstalk—L to R, R to L	V_O = 1 V_{rms}		–110		dB
I_{LIMIT}	Current limit			25		mA

(1) SNR is calculated relative to 2-Vrms output.

PW PACKAGE
(TOP VIEW)

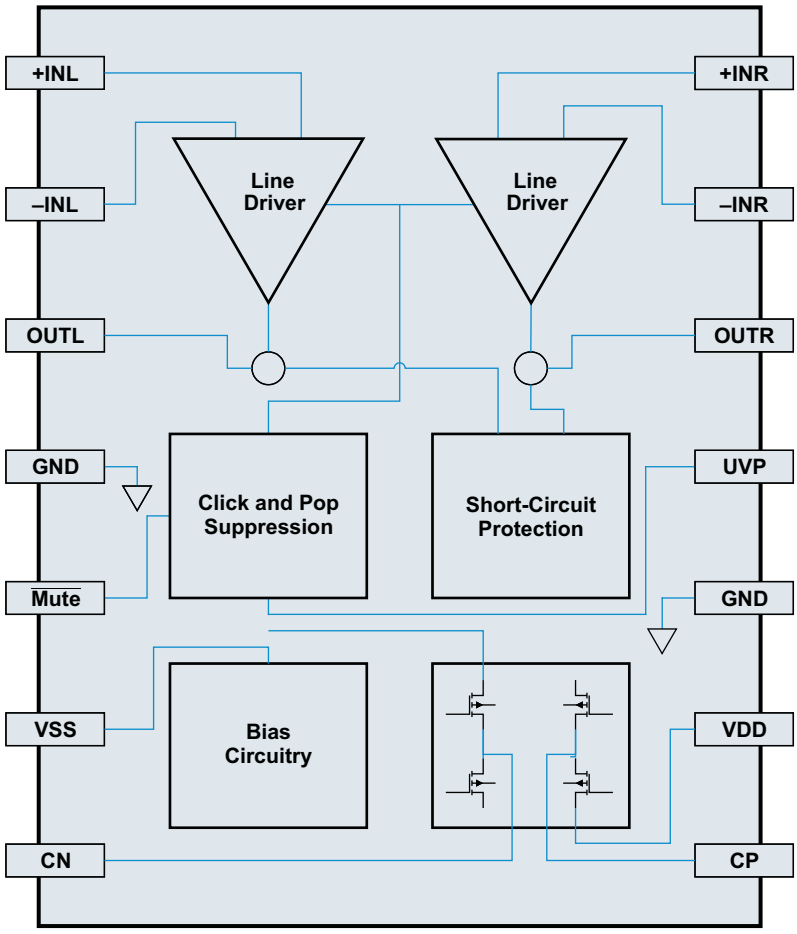


PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4, 10	P	Ground
–INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
–INR	2	I	Right-channel OPAMP negative input
+INR	1	I	Right-channel OPAMP positive input
$\overline{\text{Mute}}$	5	I	Mute, active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Undervoltage protection; connect to PVDD with a 10-kΩ resistor if function is unused.
VDD	9	P	Positive supply
VSS	6	P	Supply voltage

(1) I = input, O = output, P = power

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

VDD = 3.3 V , T_A = 25°C, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 2.2 µF, R_{IN} = 15 kΩ, R_{fb} = 30 kΩ, R_{OUT} = 32 Ω, C_{OUT} = 1 nF (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

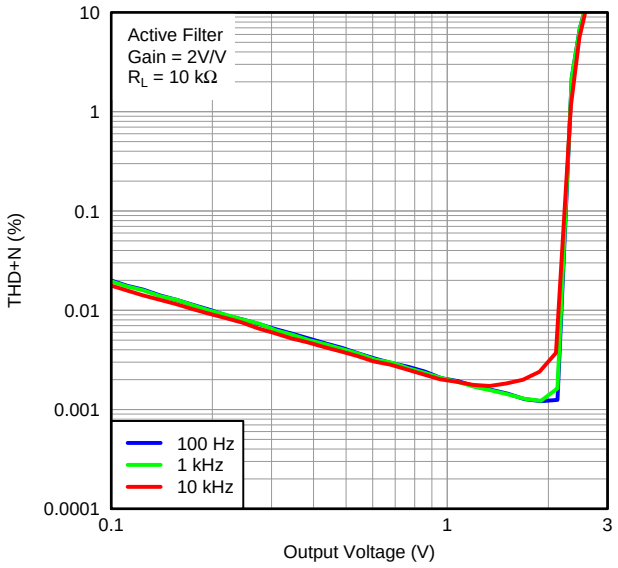


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

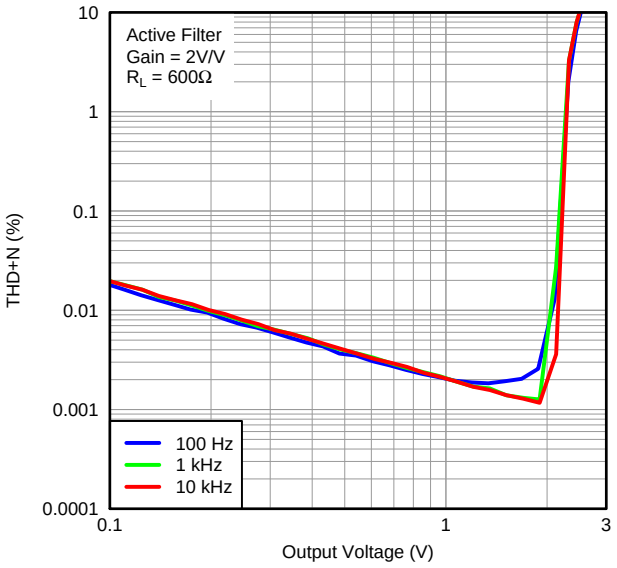


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

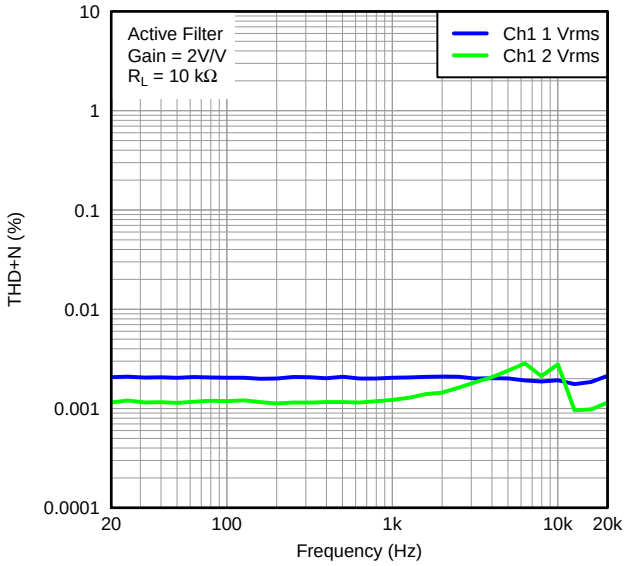


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

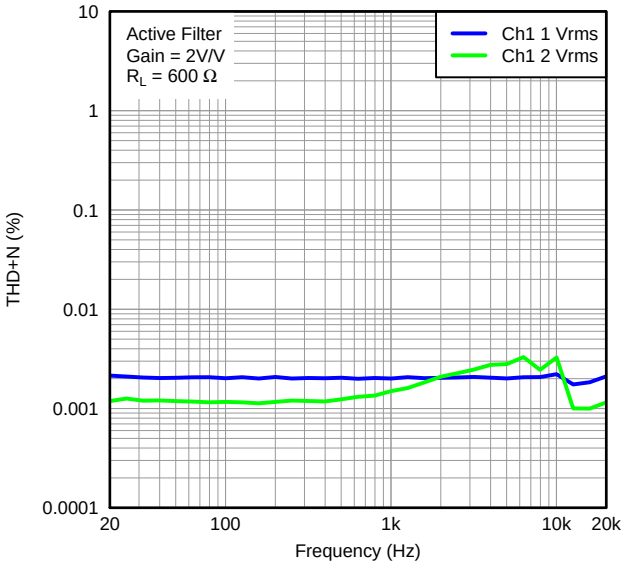


Figure 4.

TYPICAL CHARACTERISTICS (continued)

VDD = 3.3 V , T_A = 25°C, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 2.2 µF, R_{IN} = 15 kΩ, R_{fb} = 30 kΩ, R_{OUT} = 32 Ω, C_{OUT} = 1 nF (unless otherwise noted)

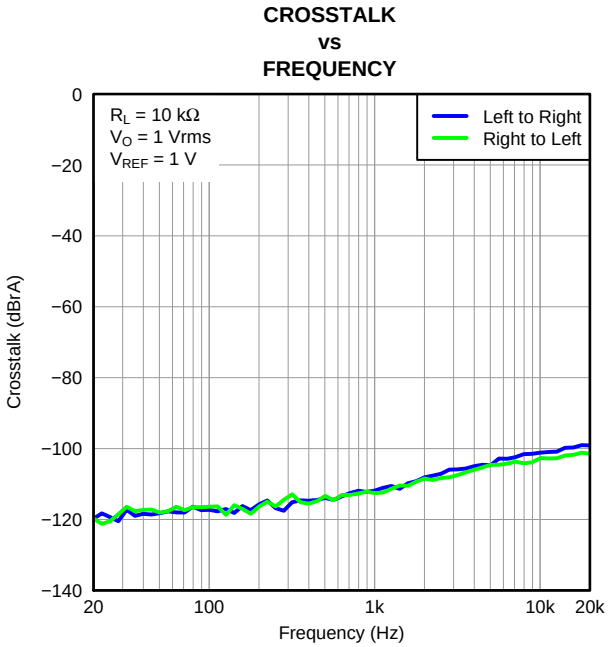


Figure 5.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 6 illustrates the conventional line-driver amplifier connection to the load and output signal. DC blocking capacitors are often large in value. The line load (typical resistive values of 600 Ω to 10 kΩ) combines with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (2)$$

If f_C is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

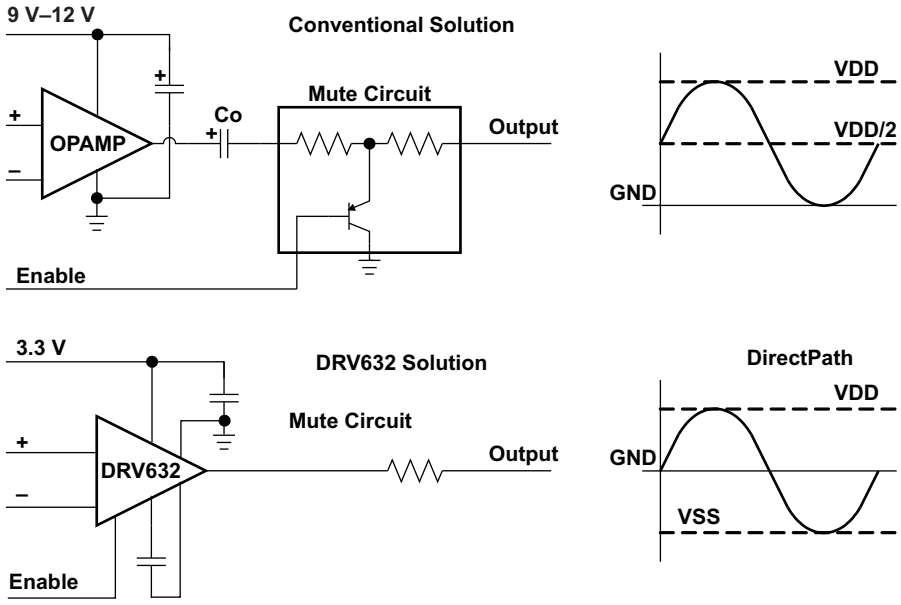


Figure 6. Conventional and DirectPath Line Drivers

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split-supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors. The bottom block diagram and waveform of Figure 6 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV632.

CHARGE-PUMP FLYING CAPACITOR AND PVSS CAPACITOR

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge-pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 μF is typical. Capacitor values that are smaller than 1 μF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications. If the DRV632 is used in highly noise-sensitive circuits, it is recommended to add a small LC filter on the VDD connection.

DECOUPLING CAPACITORS

The DRV632 is a DirectPath line-driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good, low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV632 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

GAIN-SETTING RESISTOR RANGES

The gain-setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability, and input capacitor size of the DRV632 are kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different inverting-input gain settings.

Table 1. Recommended Resistor Values

GAIN	INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}
–1 V/V	10 kΩ	10 kΩ
–1.5 V/V	8.2 kΩ	12 kΩ
–2 V/V	15 kΩ	30 kΩ
–10 V/V	4.7 kΩ	47 kΩ

USING THE DRV632 AS A SECOND-ORDER FILTER

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the DRV632, as it can be used like a standard operational amplifier. Several filter topologies can be implemented, both single-ended and differential. In Figure 7, multi-feedback (MFB) with differential input and single-ended input are shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc gain to 1, helping to reduce the output dc offset to a minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI Web site at:

http://focus.ti.com/docs/toolsw/folders/print/filterpro.html.

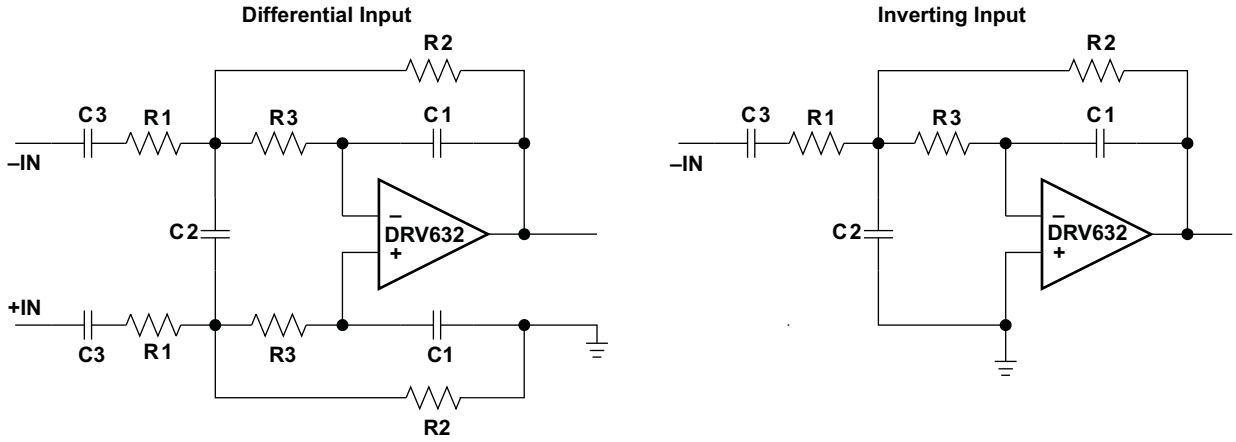


Figure 7. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small-size ac-coupling capacitor. With the proposed values of R1 = 15 kΩ, R2 = 30 kΩ, and R3 = 43 kΩ, a dynamic range (DYR) of 106 dB can be achieved with a 1-μF input ac-coupling capacitor.

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV632. These capacitors block the dc portion of the audio source and allow the DRV632 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

It is recommended to use electrolytic capacitors or high-voltage-rated capacitors as input blocking capacitors to ensure minimal variation in capacitance with input voltages. Such variation in capacitance with input voltages is commonly seen in ceramic capacitors and can increase low-frequency audio distortion.

$$f_{cIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad or \quad C_{IN} = \frac{1}{2\pi f_{cIN} R_{IN}} \tag{3}$$

DRV632 UVP OPERATION

The shutdown threshold at the UVP pin is 1.25 V. The customer must use a resistor divider to obtain the shutdown threshold and hysteresis desired for a particular application. The customer-selected thresholds can be determined as follows:

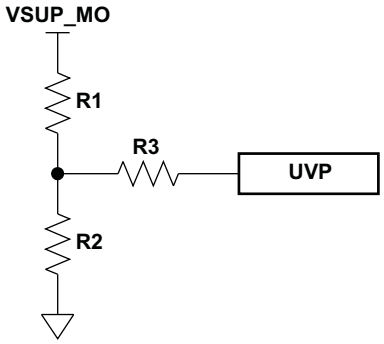
EXTERNAL UNDERVOLTAGE DETECTION

External undervoltage detection can be used to mute/shut down the DRV632 before an input device can generate a pop.

The shutdown threshold at the UVP pin is 1.25 V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

V_{UVP} = (1.25 – 6 μA × R3) × (R1 + R2) / R2
Hysteresis = 5 μA × R3 × (R1 + R2) / R2

For example, to obtain V_{UVP} = 3.8 V and 1-V hysteresis, we can use R1 = 3 kΩ, R2 = 1 kΩ, and R3 = 50 kΩ.



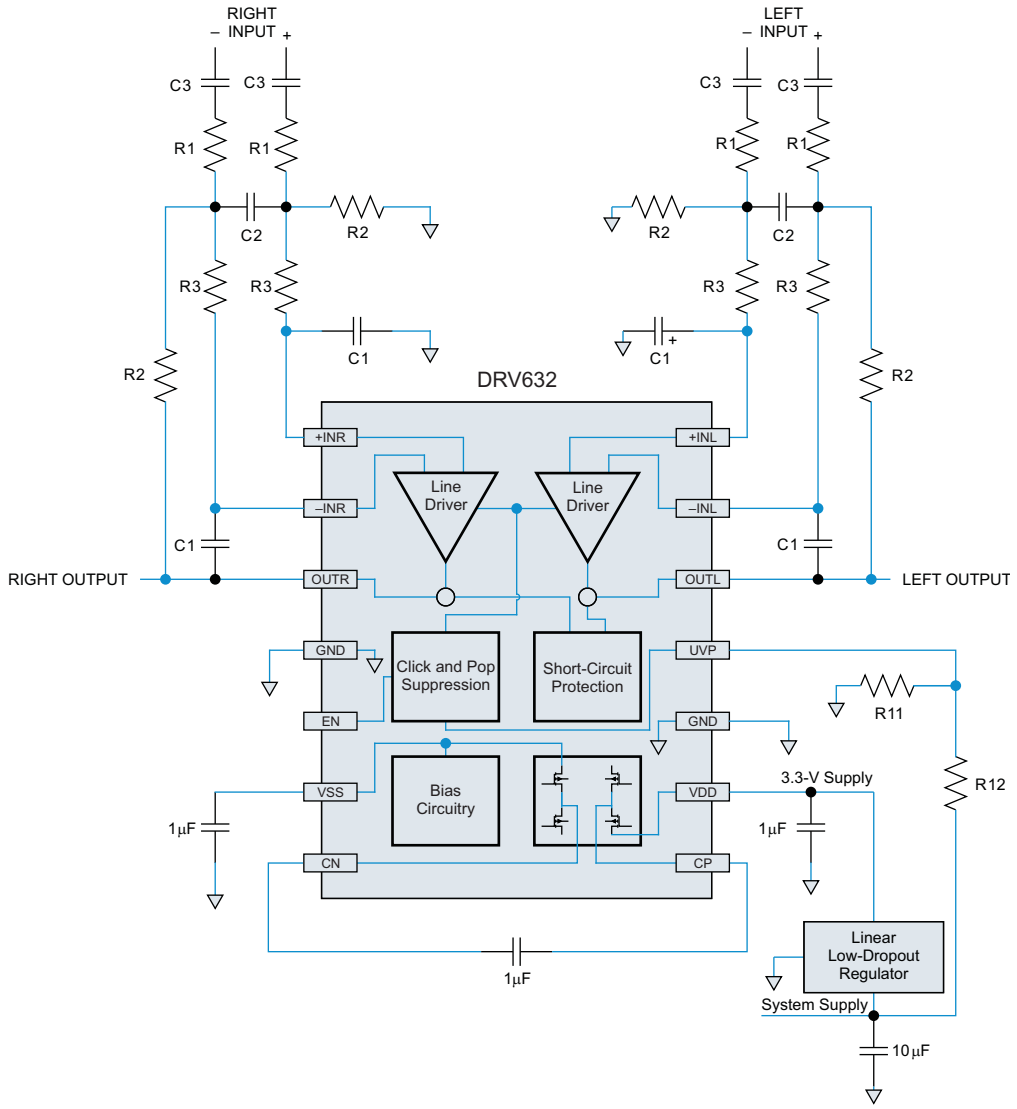
LAYOUT RECOMMENDATIONS

A proposed layout for the DRV632 can be seen in the DRV632EVM User's Guide, and the Gerber files can be downloaded from http://www.ti.com. To access this information, open the DRV632 product folder and look in the Tools and Software folder.

GAIN-SETTING RESISTORS

The gain-setting resistors, R_{IN} and R_{fb}, must be placed close to pins 13 and 17, respectively, to minimize capacitive loading on these input pins and to ensure maximum stability of the DRV632. For the recommended PCB layout, see the DRV632EVM User's Guide.

APPLICATION CIRCUIT



R1 = 15 kΩ, R2 = 30 kΩ, R3 = 43 kΩ, C1 = 47 pF, C2 = 180 pF

Differential-input, single-ended output, second-order filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV632PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
DRV632PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office

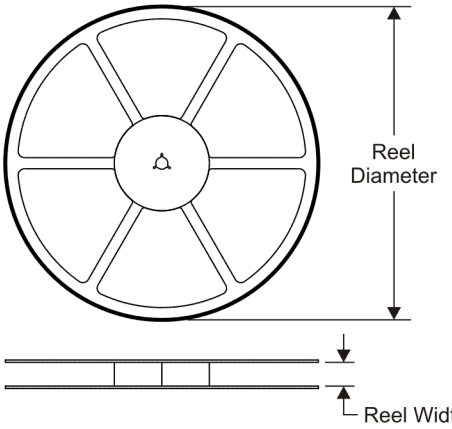
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

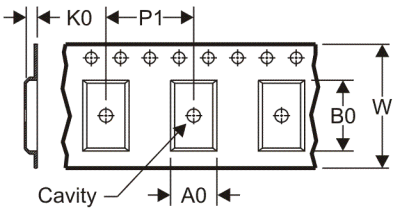
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

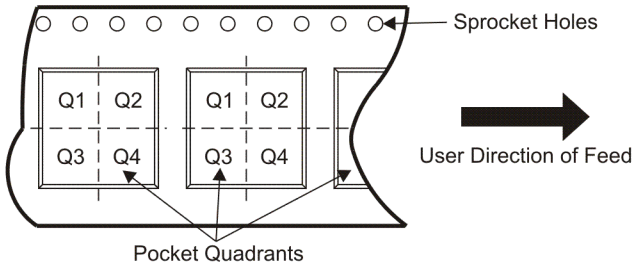


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

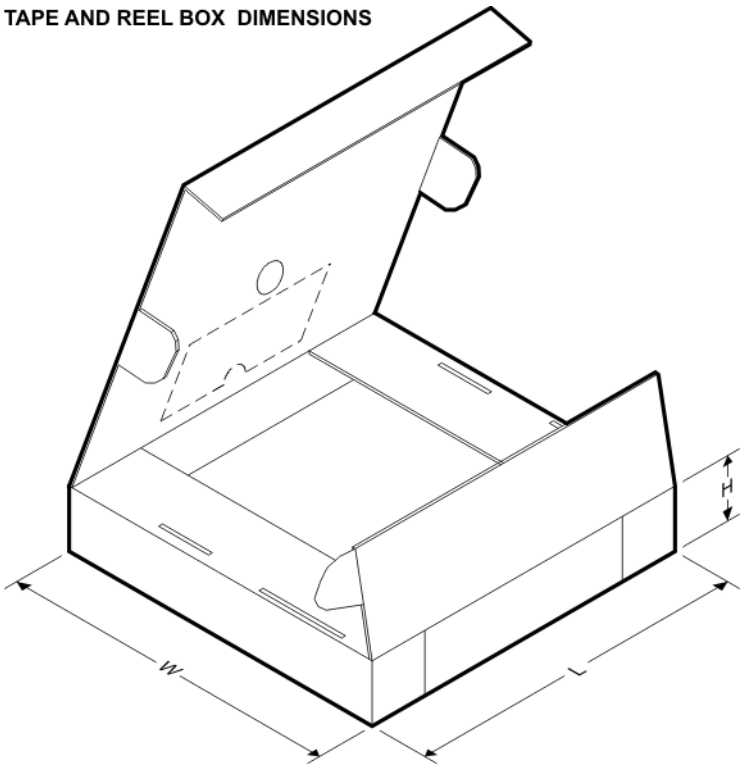
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV632PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

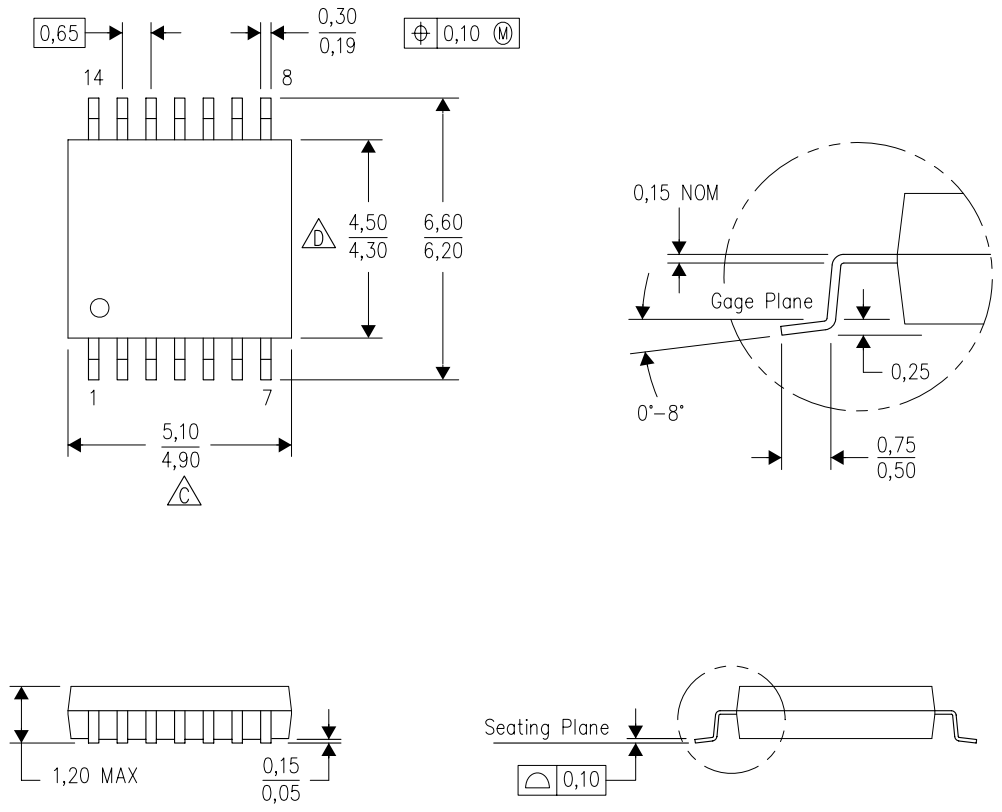
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV632PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

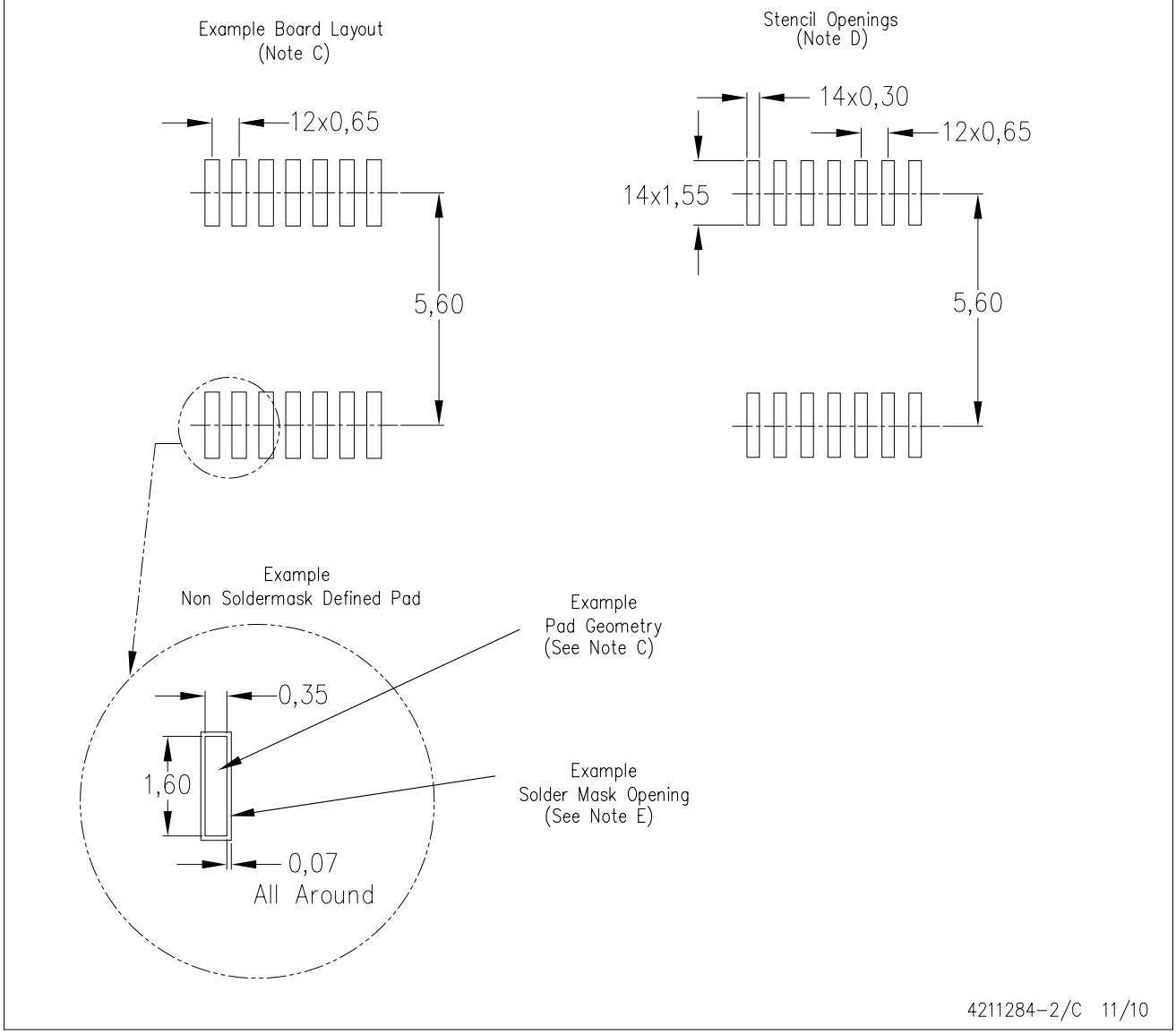
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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