Chapter 27 SPDIF Transmitter

27.1 Overview

The SPDIF transmitter is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.

It provides the basic structure of the interface. Separate documents define items specific to particular applications.

When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.

When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.

When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.

In all cases, the clock references and auxiliary information are transmitted along with the programme.

It supports following features:

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support 16, 20, 24 bits audio data transfer

27.2 Block Diagram

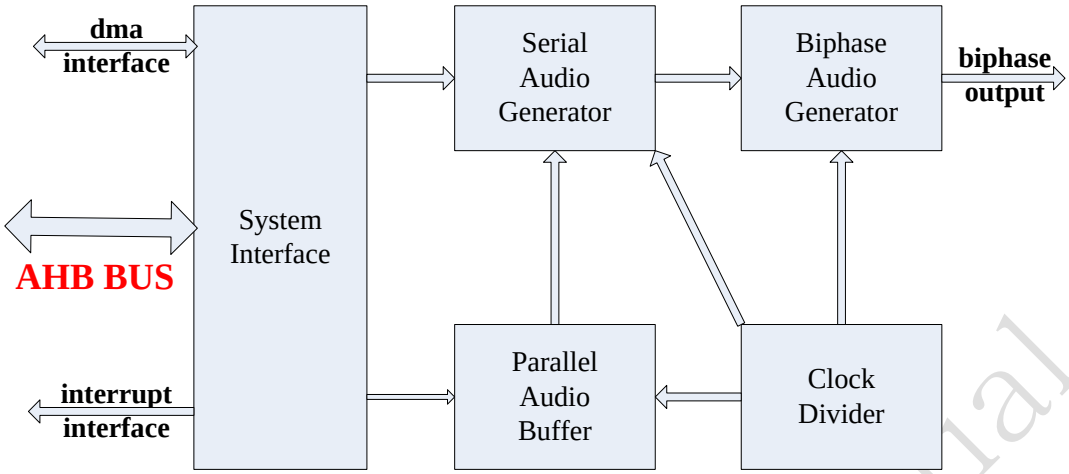

Fig.27-1SPDIF transmitter Block Diagram

The SPDIF is composed by:

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Divider

The clock divider implements clock generation function. It divides the the source clock MCLK to generate the working clock used for the digital audio data transformation and transmission.

Parallel Audio Buffer

The parallel audio buffer storesthe audio data to be transmitted. The size of the FIFO is 32bits x 32.

Serial Audio Converter

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

Biphase Audio Generator

The biphaseaudio generatorreads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

27.3 Function Description

27.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.

In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first

sub-frame(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

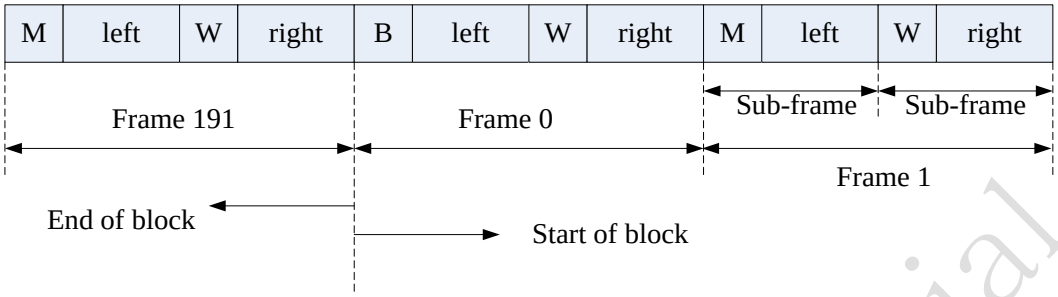

Fig.27-2SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

27.3.2 Sub-frame Format

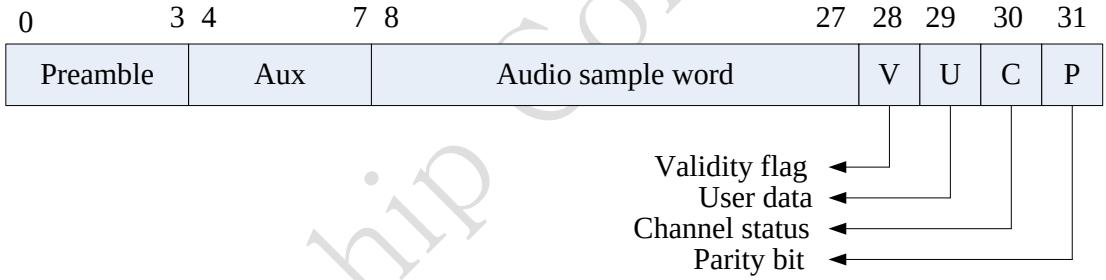

Fig.27-3SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8.Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 24 or 20),the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

27.3.3 Channel Coding

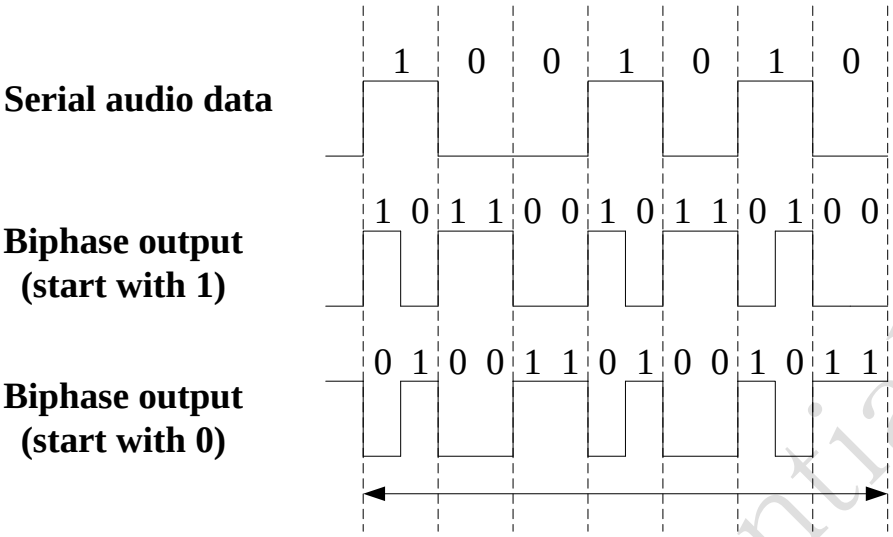

Fig.27-4SPDIF Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

27.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

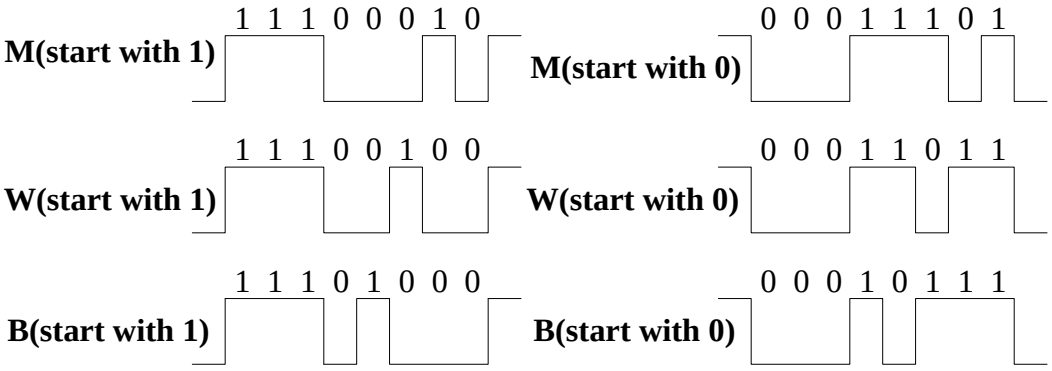

Fig.27-5SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

27.4 Register description

27.4.1 Register Summary

Name	Offset	Size	Reset value	Description
SPDIF_CFGR	0x00	W	0x0	Transfer Configuration Register
SPDIF_SDBLR	0x04	W	0x0	Sample Date Buffer Level Register
SPDIF_DMACR	0x08	W	0x0	DMA Control Register
SPDIF_INTCR	0x0C	W	0x0	Interrupt Control Register
SPDIF_INTSR	0x10	W	0x0	Interrupt Status Register
SPDIF_XFER	0x18	W	0x0	Transfer Start Register
SPDIF_SMPDR	0x20 or 0x200 ~0x3F C	W	0x0	Sample Data Register
SPDIF_VLDFR	0x60~ 0x8C	W	0x0	Validity Flag Register
SPDIF_USRDR	0x90~ 0xBC	W	0x0	User Data Register
SPDIF_CHNSR	0xC0~	W	0x0	Channel Status Register

	0xEC			

Notes:

Size: B – Byte (8 bits) access, HW – Half WORD (16 bits) access, W –WORD (32 bits) access

27.4.2 Detail Register Description

SPDIF_CFGR

Address:operationalbase+offset(0x00)

Transfer Configuration Register

Bit	Attr	Reset Value	Description
31:24	-	-	reserved
23:16	RW	0x0	MCD mclk divider Fmclk/Fsdo This parameter can be caculated by Fmclk/(Fs*128). Fs=the sample frequency be wanted
15:8	-	-	reserved
7	W	0x0	CLR mclk domain logic clear Write 1 to clear mclk domain logic. Read return zero.
6	RW	0x0	CSE Channel status enable 0: disable 1: enable
5	RW	0x0	UDE User data enable 0: disable 1: enable
4	RW	0x0	VFE Validity flag enable 0: disable 1: enable
3	RW	0x0	ADJ audio data justified The justified format of the audio data stored in FIFO. If right justified is chosen, the lower bits of the 32-bit data stored in the FIFO are valid for data sample, otherwise the higher ones are valid. 1'b0:Right justified

			1'b1:Left justified
2	RW	0x0	HWT Halfword word transform enable This bit is only valid when data width is 16-bit. When enabled, the received data from the AHB will be treated as two sets of 16bit valid data sample and stored in the same unit of the FIFO. When disabled, only the 16bit of the data is valid and stored into the FIFO. Whether higher bit or lower 16 bit is valid depends on the value of ADJ 1'b0:disable 1'b1:enable
1:0	RW	0x0	VDW Valid data width 2'b00: 16bit 2'b01：20bit 2'b10：24bit 2'b11：reserved

SPDIF_SDBLR

Address:operationalbase+offset(0x04)

Sample Date Buffer Level Register

Bit	Attr	Reset Value	Description
31:6	-	-	Reserved.
5:0	R	0x0	SDBLR Sample Date Buffer Level Register. Contains the number of valid data entries in the sample data buffer.

SPDIF_DMACR

Address:operationalbase+offset(0x08)

DMA Control Register

Bit	Attr	Reset Value	Description

31:6	-	-	Reserved.
5	RW	0x0	TDE Transmit DMA Enable 0: Transmit DMA disabled 1: Transmit DMA enabled
4:0	RW	0x0	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value

SPDIF_INTCR

Address:operationalbase+offset(0x0C)

Interrupt Control Register

Bit	Attr	Reset Value	Description
31: 17	-	-	reserved
16	W	0x0	BTTIC Block transfer terminate interrupt clear Write 1 to clear block transfer terminate interrupt.
15: 10	-	-	reserved
9:5	RW	0x0	SDBT Sample Date Buffer Threshold Sample Date Buffer Threshold for empty interrupt
4	RW	0x0	SDBEIE Sample Date Buffer empty interrupt enable 0: disable 1: enable
3	RW	0x0	BTTIE Block transfer terminate interrupt enable 0: disable 1: enable
2:0	-	-	reserved

SPDIF_INTSR

Address:operationalbase+offset(0x10)

Interrupt Status Register

Bit	Attr	Reset Value	Description
31: 5	-	-	reserved
4	R	0x0	SDBEIS Sample Date Buffer empty interrupt status 0: inactive 1: active
3	R	0x0	BTTIS Block transfer terminate interrupt status 0: inactive 1: active
2:0	-	-	Reserved.

SPDIF_XFER

Address:operationalbase+offset(0x18)

Transfer Start Register

Bit	Attr	Reset Value	Description
31: 1	-	-	Reserved.
0	RW	0x0	XFER Transfer Start Register

SPDIF_SMPDR

Address:operationalbase+offset(0x20 or 0x200 ~0x3FC)

Sample Data Register

Bit	Attr	Reset Value	Description
31:0	W	0x0	SMPDR Sample Data Register

SPDIF_VLDFR

Address:operationalbase+offset(0x60~0x8C)

Validity Flag Register

Bit	Attr	Reset Value	Description

31:0	RW	0x0	VLDFR Validity Flag Register

SPDIF_USRDR

Address:operationalbase+offset(0x90~0xBC)

User Data Register

Bit	Attr	Reset Value	Description
31:0	RW	0x0	USRDR User Data Register

SPDIF_CHNSR

Address:operationalbase+offset(0xC0~0xEC)

Channel Status Register.

Bit	Attr	Reset Value	Description
31:0	RW	0x0	CHNSR Channel Status Register

27.5 Interface description

Table 27-1 Input clock description in clock architecture diagram

Module Pin	Dir.	Pad Name	IOMUX Setting
spdif_tx	O	SPDIFtx_GPIO3d3	GRF_GPIO3D_IOMUX[6]=1'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

27.6 Application Notes

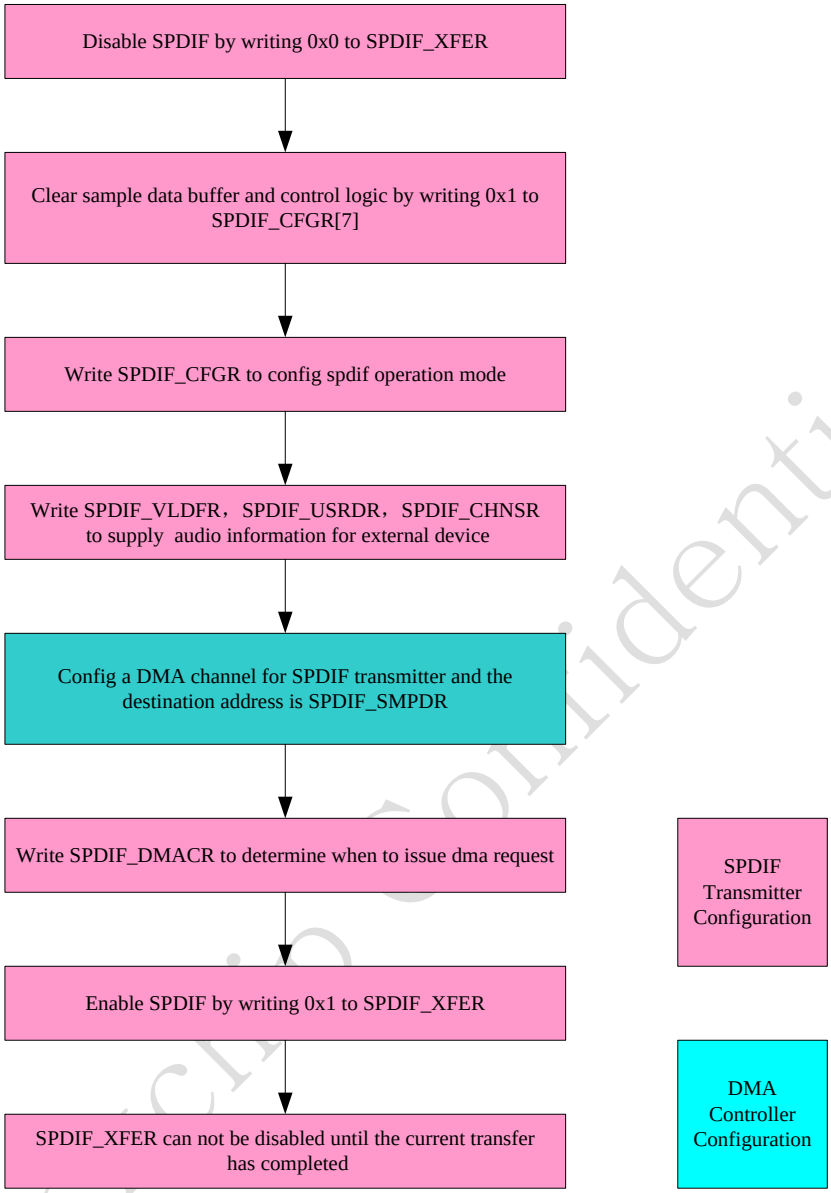

Fig.27-6 SPDIF transmitter operation flow chart

The Fig shows the operation flow of SPDIF operation. Note that the configuration register can be written only when the transfer is stopped.