# Chapter 45 MIPI Controller

## 45.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
  - 16 bits per pixel, configurations 1,2,and 3
  - 18 bits per pixel, configurations 1 and 2
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
  - Up to 2047 vertical active lines
  - Up to 63 vertical back porch lines
  - Up to 63 vertical front porch lines
  - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- All commands defined in MIPI Alliance Specification for Display Command Set (DCS)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

## 45.2 Block Diagram

The following diagram shows the MIPI Controller architecture.

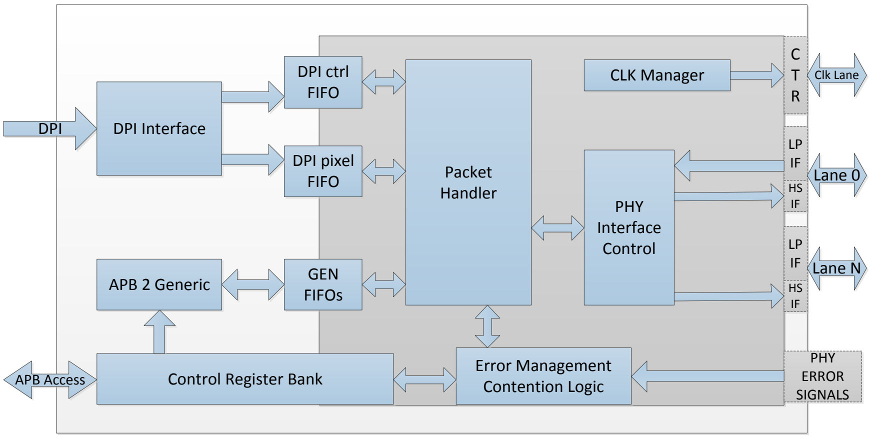



Fig. 45-1MIPI Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets, hen in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.

The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.

The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.

The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOS: Command FIFO, Write payload FIFO, Read payload FIFO.

The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

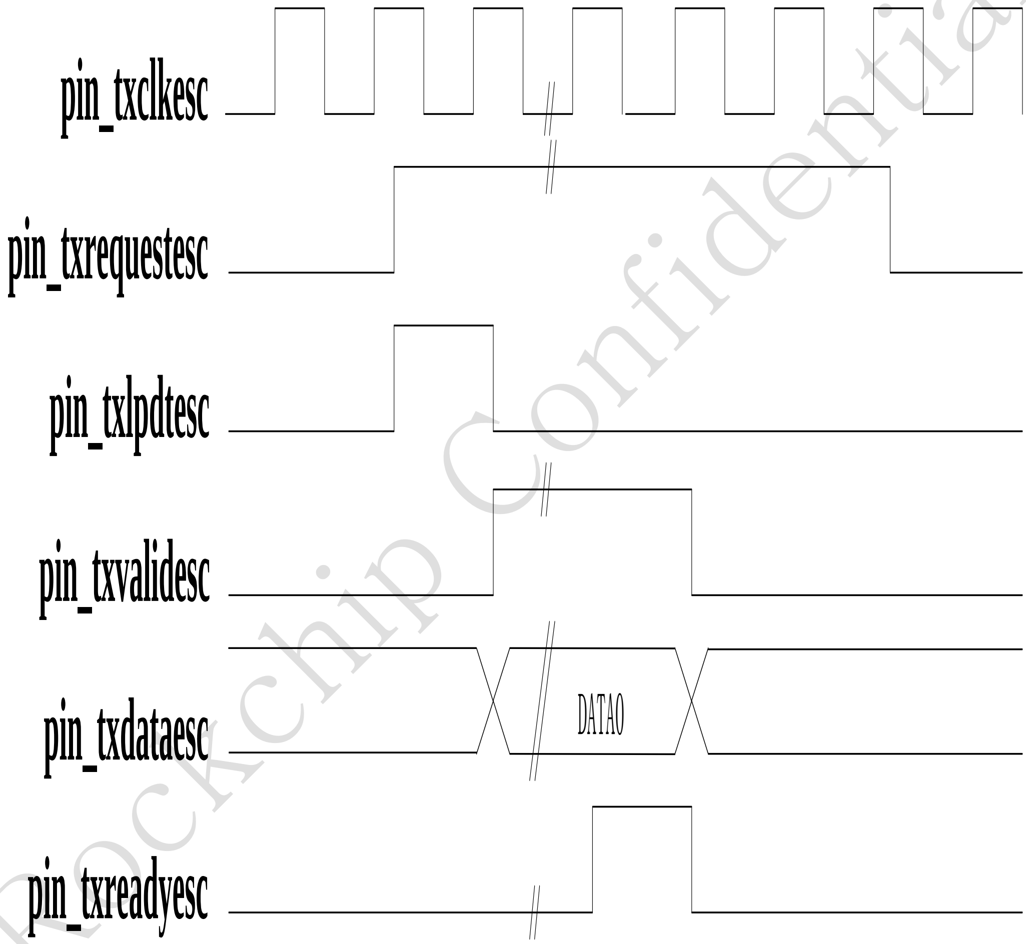
## 45.3 Function Description

### 45.3.1 DPI interface function

TheDPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of CFG_MISC_CON[2:1]. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 45-1Color table




The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows:Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.
If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the

configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

### 45.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register. The valid packets available to be transmitted through the Generic interface are as follows:
Generic Write Short Packet 0 Parameters
Generic Write Short Packet 1 Parameters
Generic Write Short Packet 2 Parameter
Generic Write Short Packet 0 Parameter
Generic Write Short Packet 1 Parameters
Generic Write Short Packet 2 Parameter
Maximum Read Packet Configuration
Generic Long Write Packet
DCS Write Short Packet 0 Parameter
DCS Write Short Packet 1 Parameter
DCS Write Short Packet 0 Parameter
DCS Write Long Packet
A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.
Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.
The transfer of packets through the APB bus is based on the following conditions:
The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.
The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bi rate achievable by the APB interface.
The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps.
The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.
To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI Controller should operate in the Command

mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.
The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least sgnificant byte position of the APB data bus.

After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be orgavized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams.In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

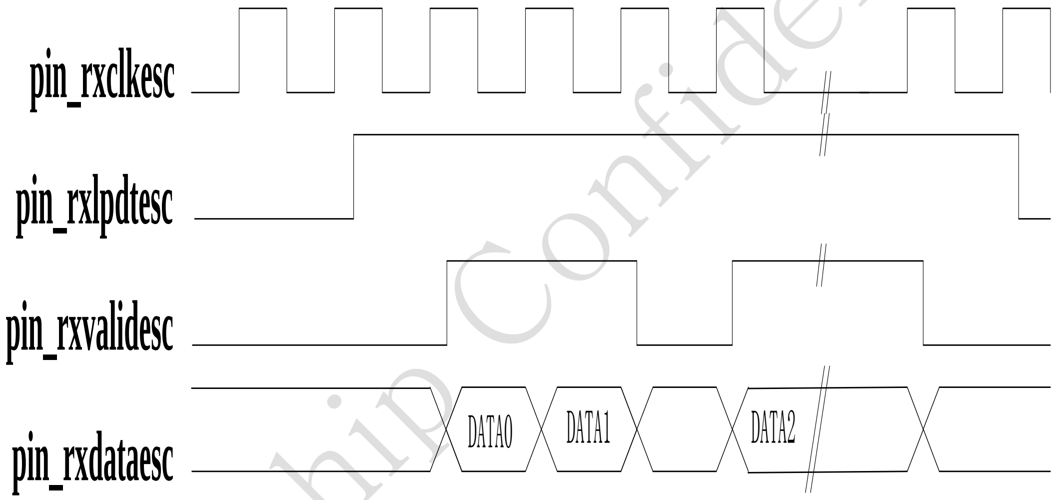



Fig. 45-224 bpp APB Pixel to Byte Organization

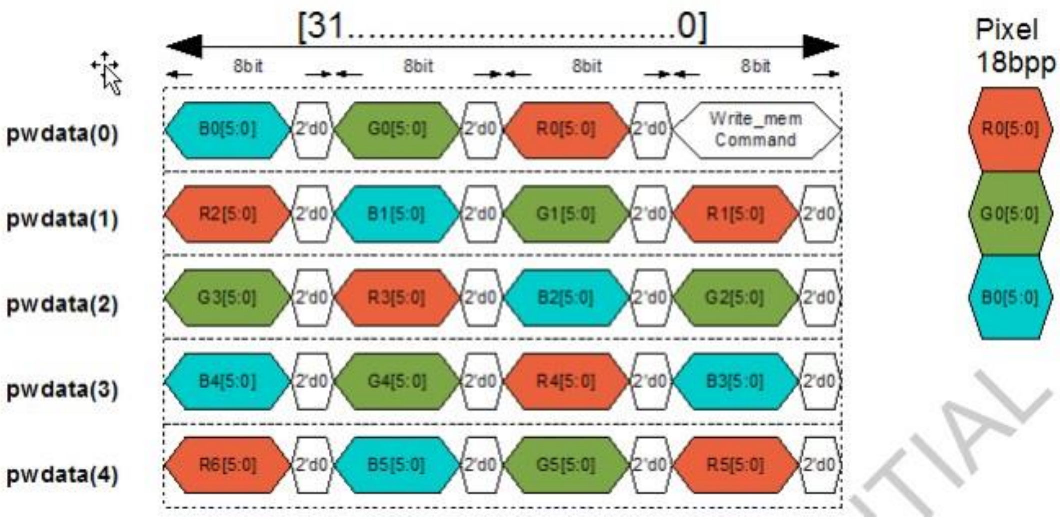


Fig. 45-318 bpp APB Pixel to Byte Organization

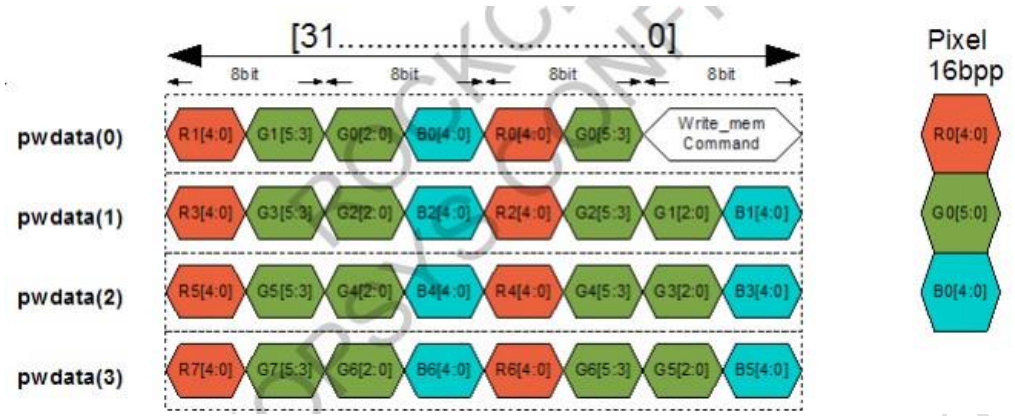



Fig. 45-416 bpp APB Pixel to Byte Organization

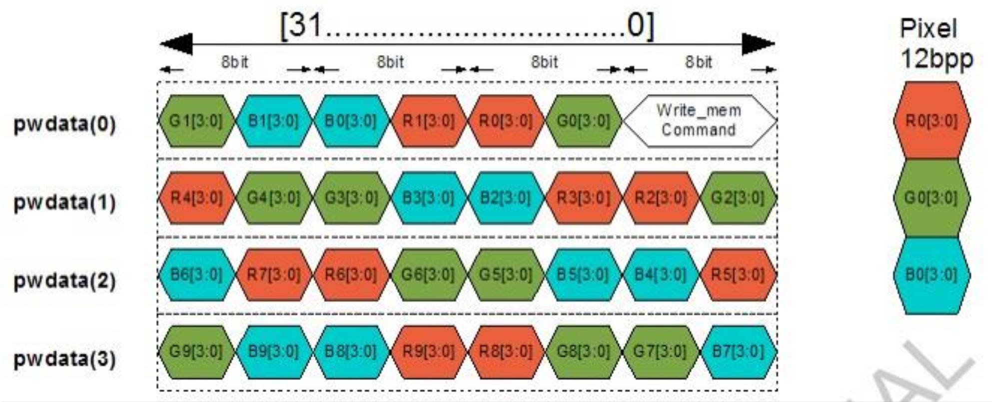



Fig. 45-512 bpp APB Pixel to Byte Organization

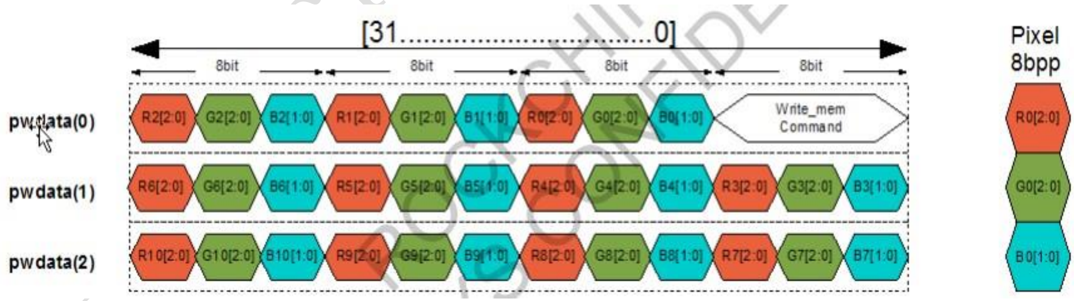



Fig. 45-68 bpp APB Pixel to Byte Organization

### 45.3.3 Transmission of Commands in Video Mode

The MIPI Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

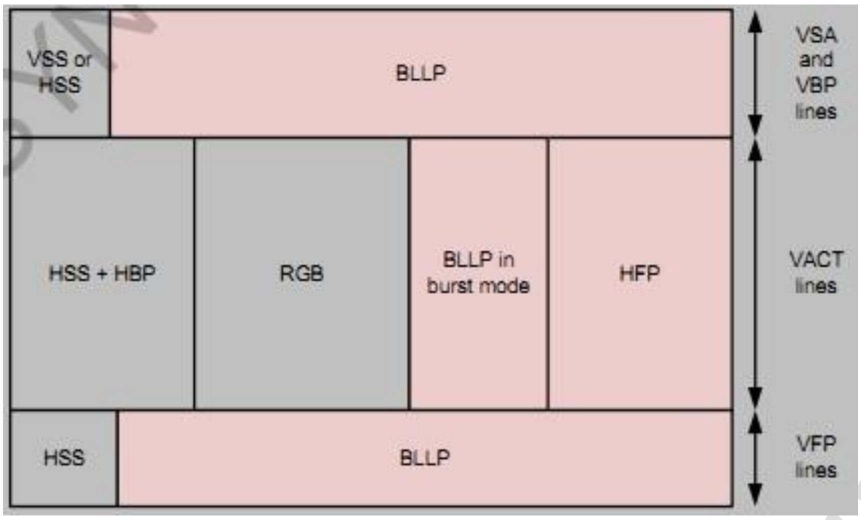



Fig. 45-7Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Bertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.
The MIPI Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) * (number of lines -1) shorter than tL.

The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DWC_mipi_dsi_host does not transmit these commands on the last line.

If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DWC_mipi_dsi_host after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).

If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical

Front Porch(VFP) regions.

The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP

*Outvact_lpcmd_time=(tL-(Time to transmit HSS and HSE frames +tHSA+Time to enter and leave LP mode+Time to send the D-PHY LPDT command)) / escape clock period / 8 / 2*

Where,

tL=Line time

tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses)

In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.

The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.

Consider an example with 12.6 µs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:

Sync pulses are not being transmitted

Two lane byte clock ticks are required to transmit a short packet

phy_lp2hs_time=16

phy_lp2p_time=20

In this example, a 11-byte command can be transmitted as follows:

outvact_lpcmd_time=(12.6µs-(2∗10 ns)-(16∗10 ns)-(20∗10 ns)-(8∗66 ns)) / 66 ns / 8 / 2 = 11 bytes

The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:

*Invact_lpcmd_time= ((tHFP-Time to enter and leave low-power mode + Blanking period before the HFP when in Burst mode- Time to send the D-PHY LPDT command) / escape clock period) / 8*

Where,

tHFP=line time-tHSA-tHBP-tHACT

tHACT=vid_pkt_size∗bits_per_pixel*lane_byte_clock_period / num_lanes

The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.

Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6µs. With a lane byte clock of 100 MHz, 1260 clock ticks are availabel to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6µs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3µs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this

period.
A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:
The controller is not in Burst mode
phy_lp2hs_time=16
phy_lp2hs_time=16
In this examplem invact_lpcmd_time is calculated as follows:
Invact_lpcmd_time = (2.3µs –(16*10 ns)-(20*10 ns)-(8*66 ns)) /66 ns / 8 = 2 bytes
The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparision to determine if a command can be transmitted in any of the BLLP periods.
Figure 5-21 illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

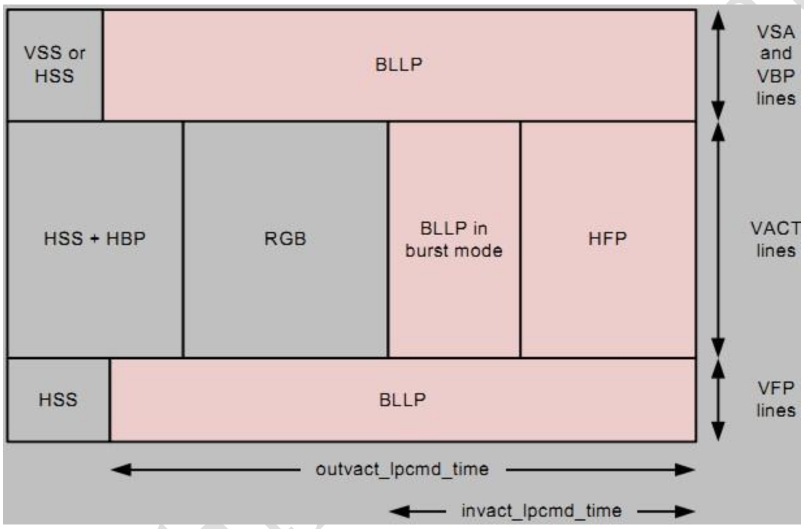



Fig. 45-8 Location of outvact_lpcmd_time and invact_lpcmd_time in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DWC_mipi_dsi_host automatically determines the area where each command can be sent and no programming or calculation is requied.

On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.
The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) =Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.
The time to return the read data packet from the pripheral depends on the number of bytes read and the escape clock frequency of the peripheal; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.
In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time + Time to return the read data packet from the peripheral device + phy_hs2hs_time

In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time +LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time
Where,
LPDT command time = (8*Host escape clock period) / Lane byte clock period
Read command time in LP mode = (32 * host escape clock period) / lane byte clock period
It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time* Lane byte clock period is less than outvact_lpcmd_time *8*Escape clock period of the host.
Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (>16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

## 45.4 Register Description

This section describes the control/status registers of the design.

### 45.4.1 Register Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| MIPIC_VERSION | 0x0000 | W | 0x3132302a | Version of the mipi controller |
| MIPIC_PWR_UP | 0x0004 | W | 0x00000000 | Core power-up |
| MIPIC_CLKMGR_CFG | 0x0008 | W | 0x00000000 | Configuration of the internal clock dividers |
| MIPIC_DPI_VCID | 0x000c | W | 0x00000000 | The DPI interface configuration. |
| MIPIC_DPI_COLOR_CODING | 0x0010 | W | 0x00000000 | |
| MIPIC_DPI_CFG_POL | 0x0014 | W | 0x00000000 | |
| MIPIC_LP_CMD_TIM | 0x0018 | W | 0x00000000 | Low-power Command Timing Configuration Register. |
| MIPIC_PCKHDL_CFG | 0x002c | W | 0x00000000 | Packet handler configuration |
| MIPIC_GEN_VCID | 0x0030 | W | 0x00000000 | |
| MIPIC_MODE_CFG | 0x0034 | W | 0x00000000 | |
| MIPIC_VID_MODE_CFG | 0x0038 | W | 0x00000000 | Video mode configuration. |
| MIPIC_VID_PKT_SIZE | 0x003c | W | 0x00000000 | |
| MIPIC_VID_NUM_CHUNKS | 0x0040 | W | 0x00000000 | |
| MIPIC_VID_NULL_SIZE | 0x0044 | W | 0x00000000 | |
| MIPIC_VID_HSA_TIME | 0x0048 | W | 0x00000000 | Line timing configuration. |
| MIPIC_VID_HBP_TIME | 0x004c | W | 0x00000000 | |
| MIPIC_VID_HLINE_TIME | 0x0050 | W | 0x00000000 | |
| MIPIC_VID_VSA_LINES | 0x0054 | W | 0x00000000 | Vertical timing configuration. |
| MIPIC_VID_VBP_LINES | 0x0058 | W | 0x00000000 | |
| MIPIC_VID_VFP_LINES | 0x005c | W | 0x00000000 | |
| MIPIC_VID_VACTIVE_LINES | 0x0060 | W | 0x00000000 | |
| MIPIC_EDPI_CMD_SIZE | 0x0064 | W | 0x00000000 | |
| MIPIC_CMD_MODE_CFG | 0x0068 | W | 0x00000000 | Command mode configuration |
| MIPIC_GEN_HDR | 0x006c | W | 0x00000000 | Generic packet header configuration. |
| MIPIC_GEN_PLD_DATA | 0x0070 | W | 0x00000000 | Generic payload data in and out. |
| MIPIC_CMD_PKT_STATUS | 0x0074 | W | 0x00000000 | Command packet status |

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| MIPIC_TO_CNT_CFG | 0x0078 | W | 0x00000000 | Timeout timers configuration |
| MIPIC_HS_RD_TO_CNT | 0x007c | W | 0x00000000 | |
| MIPIC_LP_RD_TO_CNT | 0x0080 | W | 0x00000000 | |
| MIPIC_HS_WR_TO_CNT | 0x0084 | W | 0x00000000 | |
| MIPIC_LP_WR_TO_CNT | 0x0088 | W | 0x00000000 | |
| MIPIC_BTA_TO_CNT | 0x008c | W | 0x00000000 | |
| MIPIC_LPCLK_CTRL | 0x0094 | W | 0x00000000 | |
| MIPIC_PHY_TMR_LPCLK_CFG | 0x0098 | W | 0x00000000 | |
| MIPIC_PHY_TMR_CFG | 0x009c | W | 0x00000000 | D-PHY timing configuration |
| MIPIC_PHY_RSTZ | 0x00a0 | W | 0x00000000 | D-PHY reset control |
| MIPIC_PHY_IF_CFG | 0x00a4 | W | 0x00000000 | D-PHY interface configuration |
| MIPIC_PHY_ULPS_CTRL | 0x00a8 | W | 0x00000000 | D-PHY PPI interface control |
| MIPIC_PHY_TX_TRIGGERS | 0x00ac | W | 0x00000000 | |
| MIPIC_PHY_STATUS | 0x00b0 | W | 0x00000000 | D-PHY PPI status interface |
| MIPIC_RESERVED3 | 0x00b4 | W | 0x00000000 | Reserved |
| MIPIC_RESERVED4 | 0x00b8 | W | 0x00000000 | Reserved |
| MIPIC_ERROR_ST0 | 0x00bc | W | 0x00000000 | Interrupt status register 0 |
| MIPIC_ERROR_ST1 | 0x00c0 | W | 0x00000000 | Interrupt status register 1 |
| MIPIC_MSK0 | 0x00c4 | W | 0x00000000 | Masks the interrupt generation triggerd by the ERROR_ST0 reg |
| MIPIC_MSK1 | 0x00c8 | W | 0x00000000 | Masks the interrupt generation triggerd by the ERROR_ST1 reg |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 45.4.2 Detail Register Description

**MIPIC_VERSION**
Address: Operational Base + offset (0x0000)
Version of the mipi controller

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x3132302a | version<br>indicates the version of the mipi_controller |

**MIPIC_PWR_UP**
Address: Operational Base + offset (0x0004)
Core power-up

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | shutdownz<br>This bit indicates the core power-up or the reset<br>0-Reset<br>1-Power-up |

**MIPIC_CLKMGR_CFG**
Address: Operational Base + offset (0x0008)
Configuration of the internal clock dividers

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:8 | RW | 0x00 | TO_CLK_DIVISION<br>This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error. |
| 7:0 | RW | 0x00 | TX_ESC_CLK_DIVISION<br>Field0000 Abstract<br>This field indicates the division factor for the TX_Escape clock source(lanebyteclk).The value 0 and 1 stop the TX_ESC clock generation |

**MIPIC_DPI_VCID**
Address: Operational Base + offset (0x000c)
The DPI interface configuration.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x0 | dpi_vid<br>This field configures the DPI virtual channel id that is indexed to the Video mode packets. |

**MIPIC_DPI_COLOR_CODING**
Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | en18_loosely<br>When set to 1,this bit enables 18 loosely packed pixel stream. |
| 7:4 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | dpi_color_coding<br>This field configures the DPI color coding as follows:<br>000:16bit configuration 1<br>001:16bit configuration 2<br>010:16bit configuration 3<br>011:18bit configuration 1<br>100:18bit configuration 2<br>101,110,and 111:24bits |

**MIPIC_DPI_CFG_POL**
Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | colorm_active_low<br>When set to 1,this bit configures the color mode pin as active low |
| 3 | RW | 0x0 | shutd_active_low<br>When set to 1,this bit configures the shut down pin as active low |
| 2 | RW | 0x0 | hsync_active_low<br>When set to 1,this bit configures the horizontal synchronism pin as active low. |
| 1 | RW | 0x0 | vsync_active_low<br>When set to 1,this bit configures the vertical synchronism pin as active low |
| 0 | RW | 0x0 | dataen_active_low<br>When set to 1,this bit configures the data enable pin as active low |

**MIPIC_LP_CMD_TIM**
Address: Operational Base + offset (0x0018)
Low-power Command Timing Configuration Register.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | reserved |
| 23:16 | RW | 0x00 | outvact_lpcmd_time<br>outside VACT region command time.This field configures the time available to transmit a command in low-power mode.The time value is expressed in a number of bytes format.The number of bytes represents the maximum size of a packet that can fit in a line during the VSA,VBP,and VFP region.<br>This field must be configured with a value greater than or equal to four bytes to allow the transmission of the DCTRL commands such as shutdown and colorm in low-power mode. |
| 15:8 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | invact_lpcmd_time<br>Inside VACT region command time.This field configures the time available to transmit a command in low-power mode.The time value is expressed in a number of bytes format.The number of bytes represents the maximum size of the packet that can fit a line during the VACT region. |

**MIPIC_PCKHDL_CFG**
Address: Operational Base + offset (0x002c)
Packet handler configuration

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | en_CRC_rx<br>When set to 1,this bit enables the CRC reception and error reporting |
| 3 | RW | 0x0 | en_ECC_rx<br>When set to 1,this bit enables the ECC reception,error correction,and reporting |
| 2 | RW | 0x0 | en_BTA<br>When set to 1,this bit enables the Bus Turn-Around(BTA) request. |
| 1 | RW | 0x0 | en_EOTp_rx<br>When set to 1,this bit enables the EOTp reception |
| 0 | RW | 0x0 | en_EOTp_tx<br>When set to 1,this bit enables the EOTp transmission |

**MIPIC_GEN_VCID**
Address: Operational Base + offset (0x0030)
Packet handler configuration

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x0 | gen_vid_rx<br>This field indicates the Generic interface read-back virtual channel identification |

**MIPIC_MODE_CFG**
Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | en_video_mode<br>When set to 1,this bit enables the DPI Video mode transmission. |

**MIPIC_VID_MODE_CFG**
Address: Operational Base + offset (0x0038)
Video mode configuration.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15 | RW | 0x0 | lpcmden<br>When set to 1,this bit enables the command transmission only in low-power mode |
| 14 | RW | 0x0 | frame_BTA_ack<br>When set to 1,this bit enables the request for an acknowledge response at the end of a frame |
| 13 | RW | 0x0 | en_lp_hfp<br>When set to 1,this bit enables the return to low-power inside the HFP period when timing allows. |
| 12 | RW | 0x0 | en_lp_hbp<br>When set to 1,this bit enables the return to low-power inside the HBP period when timing allows. |
| 11 | RW | 0x0 | en_lp_vact<br>When set to 1,this bit enables the return to low-power inside the VACT period when timing allows. |
| 10 | RW | 0x0 | en_lp_vfp<br>When set to 1,this bit enables the return to low-power inside the VFP period when timing allows. |
| 9 | RW | 0x0 | en_lp_vbp<br>When set to 1,this bit enables the return to low-power inside the VBP period when timing allows. |
| 8 | RW | 0x0 | en_lp_vsa<br>When set to 1,this bit enables the return to low-power inside the VSA period when timing allows. |
| 7:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x0 | vid_mode_type<br>This field indicates the video mode transmission type as follows:<br>00:Non-burst with sync pulses<br>01:Non-burst with sync events<br>10 and 11:Burst with sync pulses |

**MIPIC_VID_PKT_SIZE**
Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | vid_pkt_size<br>This field configures the number of pixels on a single vedio packet.if you use the 18-bit mode and do not enable loosely packed stream,this vaule must be a multiple of 4. |

**MIPIC_VID_NUM_CHUNKS**
Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | num_chunks<br>This field configures the number of chunks to be transmitted during a line period(a chunk is a video packet or a null packet) |

**MIPIC_VID_NULL_SIZE**
Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | null_pkt_size<br>This field configures the number of bytes in a null packet |

**MIPIC_VID_HSA_TIME**
Address: Operational Base + offset (0x0048)
Line timing configuration.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x0 | reserved |
| 11:0 | RW | 0x000 | hsa_time<br>This field configures the Horizontal Synchronism Active period in lane byte clock cycles. |

**MIPIC_VID_HBP_TIME**
Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x0 | reserved |
| 11:0 | RW | 0x000 | hbp_time<br>This field configures the Horizontal Back Porch period in lane byte clock cycles |

**MIPIC_VID_HLINE_TIME**
Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x0 | reserved |
| 14:0 | RW | 0x0000 | hline_time<br>This field configures the size of the total lines counted in lane byte cycles. |

**MIPIC_VID_VSA_LINES**
Address: Operational Base + offset (0x0054)
Vertical timing configuration.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | reserved |
| 9:0 | RW | 0x000 | vsa_lines<br>This field configures the Vertical Synchronism Active period measured in number of horizontal lines. |

**MIPIC_VID_VBP_LINES**
Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | reserved |
| 9:0 | RW | 0x000 | vbp_lines<br>This field configures the Vertical Back Porch period measured in horizontal lines. |

**MIPIC_VID_VFP_LINES**
Address: Operational Base + offset (0x005c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | reserved |
| 9:0 | RW | 0x000 | vfp_lines<br>This field configures the Vertical Front Porch period measured in horizontal lines. |

**MIPIC_VID_VACTIVE_LINES**
Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | v_active_line<br>This field configures the Vertical Active period measured in horizontal lines. |

**MIPIC_EDPI_CMD_SIZE**
Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | edpi_allowed_cmd_size<br>This field configures the maximum allowed size for an eDPI write memory command,measured in pixels.Automatic partitioning of data obtained from eDPI is permanently enabled. |

**MIPIC_CMD_MODE_CFG**
Address: Operational Base + offset (0x0068)
Command mode configuration

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | reserved |
| 24 | RW | 0x0 | max_rd_pkt_size<br>This bit configures the maximum read packet size command transmission type:<br>0:High-speed<br>1:Low-power |
| 23:20 | RO | 0x0 | reserved |
| 19 | RW | 0x0 | dcs_lw_tx<br>This bit configures the DCS long write packet command transmission type:<br>0:High-speed<br>1:Low-power |
| 18 | RW | 0x0 | dcs_sr_0p_tx<br>This bit configures the DCS short read packet with zero parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 17 | RW | 0x0 | dcs_sw_1p_tx<br>This bit configures the DCS short write packet with one parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 16 | RW | 0x0 | dcs_sw_0p_tx<br>This bit configures the DCS short write packet with zero parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | gen_lw_tx<br>This bit configures the Generic long write packet command<br>0:High-speed<br>1:Low-power |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | gen_sr_2p_tx<br>This bit configures the Generic short read packet with two parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 12 | RW | 0x0 | gen_sr_1p_tx<br>This bit configures the Generic short read packet with one parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 11 | RW | 0x0 | gen_sr_0p_tx<br>This bit configures the Generic short read packet with zero parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 10 | RW | 0x0 | gen_sw_2p_tx<br>This bit configures the Generic short write packet with two parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 9 | RW | 0x0 | gen_sw_1p_tx<br>This bit configures the Generic short write packet with one parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 8 | RW | 0x0 | gen_sw_0p_tx<br>This bit configures the Generic short write packet with zero parameter command transmission type:<br>0:High-speed<br>1:Low-power |
| 7:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | ack_rqst_en<br>When |
| 0 | RW | 0x0 | tear_fx_en<br>When set to 1,this bit enables the tearing effect acknowledge request |

**MIPIC_GEN_HDR**
Address: Operational Base + offset (0x006c)
Generic packet header configuration.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | gen_WC_MSbyte<br>This field configures the most significant byte of the header packet's Word count for long packets or data 1 for short packets. |
| 15:8 | RW | 0x00 | gen_WC_LSbyte<br>This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets. |
| 7:6 | RW | 0x0 | gen_VC<br>This field configures the virtual channel id of the header packet. |
| 5:0 | RW | 0x00 | gen_DT<br>This field configures the packet data type of the header packet |

**MIPIC_GEN_PLD_DATA**
Address: Operational Base + offset (0x0070)
Generic payload data in and out.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | gen_pld_b4<br>This field indicates byte 4 of the packet payload. |
| 23:16 | RW | 0x00 | gen_pld_b3<br>This field indicates byte 3 of the packet payload. |
| 15:8 | RW | 0x00 | gen_pld_b2<br>This field indicates byte 2 of the packet payload. |
| 7:0 | RW | 0x00 | gen_pld_b1<br>This field indicates byte 1 of the packet payload. |

**MIPIC_CMD_PKT_STATUS**
Address: Operational Base + offset (0x0074)
Command packet status

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | reserved<br>reserved |
| 6 | RW | 0x0 | gen_rd_cmd_busy<br>This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO |
| 5 | RW | 0x0 | gen_pld_r_full<br>This bit indicates the full status of the generic read payload FIFO<br>Vaule after reset:0x0 |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x0 | gen_pld_r_empty<br>This bit indicates the empty status of the generic read payload FIFO<br>Vaule after reset:0x1 |
| 3 | RO | 0x0 | gen_pld_w_full<br>This bit indicates the full status of the generic write payload FIFO<br>Vaule after reset:0x0 |
| 2 | RO | 0x0 | gen_pld_w_empty<br>This bit indicates the empty status of the generic write payload FIFO<br>Vaule after reset:0x1 |
| 1 | RO | 0x0 | gen_cmd_full<br>This bit indicates the full status of the generic command FIFO<br>Vaule after reset:0x0 |
| 0 | RO | 0x0 | gen_cmd_empty<br>This bit indicates the empty status of the generic command FIFO<br>Vaule after reset:0x1 |

**MIPIC_TO_CNT_CFG**
Address: Operational Base + offset (0x0078)
Timeout timers configuration

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | hstx_to_cnt<br>This field configures the timeout counter that triggers a high-speed transmission timeout contention detection(measured in TO_CLK_DIVISION cycles) |
| 15:0 | RW | 0x0000 | lprx_to_cnt<br>This field configures the timeout counter that triggers a low-power reception timeout contention detection(measured in TO_CLK_DIVISION cycles) |

**MIPIC_HS_RD_TO_CNT**
Address: Operational Base + offset (0x007c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | hs_rd_to_cnt<br>This field sets a period for which the MIPI Controller keeps the link still,after sending a high-speed read operation.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts. |

**MIPIC_LP_RD_TO_CNT**
Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | lp_rd_to_cnt<br>This field sets a period for which MIPI Controller keeps the link still,after sending a low-power read operation.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts. |

**MIPIC_HS_WR_TO_CNT**
Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | reserved |
| 24 | RW | 0x0 | presp_to_mode<br>When set to 1, this bit ensures that the peripheral respone timeout caused by hs_wr_to_cnt is used only once per eDPI frame,when both the following conditions are met:<br>.dpivsync_edpiwms has risen and fallen<br>.packets originated from eDPI have been transmitted and its FIFO is empty again. |
| 23:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | hs_wr_to_cnt<br>This field sets a period for which the MIPI Controller keeps the link inactive after sending a high-speed write operation.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts. |

**MIPIC_LP_WR_TO_CNT**
Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0 | lp_wr_to_cnt<br>This field sets a period for which the DSI Controller keeps the link still,after sending a low-power write operation.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts. |

**MIPIC_BTA_TO_CNT**

Address: Operational Base + offset (0x008c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | bta_to_cnt<br>This field sets a period for which the DSI Controller keeps the link still,after completing a Bus Turn-Around.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts. |

**MIPIC_LPCLK_CTRL**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | auto_clklane_ctrl<br>This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows. |
| 0 | RW | 0x0 | phy_txrequestclkhs<br>This bit controls the D-PHY PPI tx requestclkhs signal |

**MIPIC_PHY_TMR_LPCLK_CFG**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x0 | reserved |
| 25:16 | RW | 0x000 | phy_hs2lp_time<br>This field configures the maximum time that the PHY takes to go from high-speed to low-power transmission measured in lane byte clock cycles.(clock lane) |
| 15:10 | RO | 0x0 | reserved |
| 9:0 | RW | 0x000 | phy_lp2hs_time<br>This field configures the maximum time that the PHY takes to go from low-power to high-speed transmission measured in lane byte clock cycles.(clock lane) |

**MIPIC_PHY_TMR_CFG**

Address: Operational Base + offset (0x009c)

D-PHY timing configuration

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | phy_hs2lp_time<br>This field configures the maximum time that the PHY takes to go from high-speed to low-power transmission measured in lane byte clock cycles. |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | phy_lp2hs_time<br>This field configures the maximum time that the PHY takes to go from low-power to high-speed transmission measured in lane byte clock cycles. |
| 15 | RW | 0x0 | reserved<br>reserved for future use |
| 14:0 | RW | 0x0000 | max_rd_time<br>This field configures the maximum time required to perform a read command in lane byte clock cycles.This register can only by modified when read commands are not in progress. |

**MIPIC_PHY_RSTZ**
Address: Operational Base + offset (0x00a0)
D-PHY reset control

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | phy_enableclk<br>When set to 1,this bit enables the D-PHY Clock Lane Module |
| 1 | RW | 0x0 | reserved1 |
| 0 | RW | 0x0 | reserved |

**MIPIC_PHY_IF_CFG**
Address: Operational Base + offset (0x00a4)
D-PHY interface configuration

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:8 | RW | 0x00 | phy_stop_wait_time<br>This field configures the minimum wait period to request a high-speed transmission after the Stop state is accounted in clock lane cycles. |
| 7:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x0 | n_lanes<br>This field configures the number of active data lanes:<br>00:One data lane(lane 0)<br>01:Two data lane(lanes 0 and 1)<br>10:Three data lanes(lanes 0,1,and 2)<br>11:Four data lanes(lanes 0,1,2,and 3) |

**MIPIC_PHY_ULPS_CTRL**
Address: Operational Base + offset (0x00a8)
D-PHY PPI interface control

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | phy_txexitulpslan<br>ULPS mode Exit on all active data lanes |
| 2 | RW | 0x0 | phy_txrequlpslan<br>ULPS mode Request on all active data lanes |
| 1 | RW | 0x0 | phy_txexitulpsclk<br>ULPS mode Exit on clock lane |
| 0 | RW | 0x0 | phy_txrequlpsclk<br>ULPS mode Request on clock lane |

**MIPIC_PHY_TX_TRIGGERS**
Address: Operational Base + offset (0x00ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | phy_tx_triggers<br>This field controls the trigger transmissions. |

**MIPIC_PHY_STATUS**
Address: Operational Base + offset (0x00b0)
D-PHY PPI status interface

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0 | reserved |
| 12 | RO | 0x0 | ulpsactivenot3lane<br>This bit indicates the status of ulpsactivenot3lane D-PHY signal |
| 11 | RO | 0x0 | phystopstate3lane<br>This bit indicates the status of phystopstate3lane D-PHY signal |
| 10 | RO | 0x0 | ulpsactivenot2lane<br>This bit indicates the status of ulpsactivenot2lane D-PHY signal |
| 9 | RO | 0x0 | phystopstate2lane<br>This bit indicates the status of phystopstate2lane D-PHY signal |
| 8 | RO | 0x0 | ulpsactivenot1lane<br>This bit indicates the status of ulpsactivenot1lane D-PHY signal |
| 7 | RO | 0x0 | phystopstate1lane<br>This bit indicates the status of phystopstate1lane D-PHY signal |
| 6 | RW | 0x0 | rxulpsesc0lane<br>This bit indicates the status of rxulpsesc0lane D-PHY signal |
| 5 | RO | 0x0 | ulpsactivenot0lane<br>This bit indicates the status of ulpsactivenot0lane D-PHY signal |
| 4 | RO | 0x0 | phystopstate0lane<br>This bit indicates the status of phystopstate0lane D-PHY signal |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | phyulpsactivenotclk<br>This bit indicates the status of phyulpsactivenotclk D-PHY signal |
| 2 | RO | 0x0 | phystopstateclklane<br>This bit indicates the status of phystopstateclklane D-PHY signal |
| 1 | RO | 0x0 | phydirection<br>This bit indicates the status of phydirection D-PHY signal |
| 0 | RO | 0x0 | phylock<br>This bit indicates the status of phylock D-PHY signal |

**MIPIC_RESERVED3**
Address: Operational Base + offset (0x00b4)
Reserved

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | Reserved |

**MIPIC_RESERVED4**
Address: Operational Base + offset (0x00b8)
Reserved

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | Reserved |

**MIPIC_ERROR_ST0**
Address: Operational Base + offset (0x00bc)
Interrupt status register 0

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x0 | reserved |
| 20 | RO | 0x0 | dphy_errors_4<br>This bit indicates LP1 contention error ErrContentionLP1 from Lane 0 |
| 19 | RO | 0x0 | dphy_errors_3<br>This bit indicates LP0 contention error ErrContentionLP0 from Lane 0 |
| 18 | RO | 0x0 | dphy_errors_2<br>This bit indicates control error ErrControl from Lane 0 |
| 17 | RO | 0x0 | dphy_errors_1<br>This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0 |
| 16 | RO | 0x0 | dphy_errors_0<br>This bit indicates ErrEsc escape entry error from Lane 0 |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RO | 0x0 | ack_with_err_15<br>This bit retrieves the DSI protocol violation from the Display Acknowledge error report |
| 14 | RO | 0x0 | ack_with_err_14<br>This bit retrieves the reserved(specific to device) from the Display Acknowledge error report |
| 13 | RO | 0x0 | ack_with_err_13<br>This bit retrieves the invalid transmission length from the Display Acknowledge error report |
| 12 | RO | 0x0 | ack_with_err_12<br>This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report |
| 11 | RO | 0x0 | ack_with_err_11<br>This bit retrieves the not recognized DSI data type from the Display Acknowledge error report |
| 10 | RO | 0x0 | ack_with_err_10<br>This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report |
| 9 | RO | 0x0 | ack_with_err_9<br>This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report |
| 8 | RO | 0x0 | ack_with_err_8<br>This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report |
| 7 | RO | 0x0 | ack_with_err_7<br>This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report |
| 6 | RO | 0x0 | ack_with_err_6<br>This bit retrieves the False Control error from the Display Acknowledge error report |
| 5 | RO | 0x0 | ack_with_err_5<br>This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report |
| 4 | RO | 0x0 | ack_with_err_4<br>This bit retrieves the LP Transmit Sync error error from the Display Acknowledge error report |
| 3 | RO | 0x0 | ack_with_err_3<br>This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report |
| 2 | RO | 0x0 | ack_with_err_2<br>This bit retrieves the EoT sync error from the Display Acknowledge error report |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | ack_with_err_1<br>This bit retrieves the SoT Sync error from the Display Acknowledge error report |
| 0 | RO | 0x0 | ack_with_err_0<br>This bit retrieves the SoT error from the Display Acknowledge error report |

**MIPIC_ERROR_ST1**
Address: Operational Base + offset (0x00c0)
Interrupt status register 1

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0 | reserved |
| 12 | RO | 0x0 | gen_pld_recv_err<br>This bit indicates that during a generic interface packet read back,the payload FIFO becomes full and the received data is corrupted. |
| 11 | RO | 0x0 | gen_pld_rd_err<br>This bit indicates that during a DCS read data,the payload FIFO becomes empty and the data sent to the interface is corrupted |
| 10 | RO | 0x0 | gen_pld_send_err<br>This bit indicates that during a Generic interface packet build,the payload FIFO becomes empty and corrupt data is sent. |
| 9 | RO | 0x0 | gen_pld_wr_err<br>This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full.Therefore,the command is not written. |
| 8 | RO | 0x0 | gen_cmd_wr_err<br>This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full.Therefore,the command is not written. |
| 7 | RO | 0x0 | dpi_pld_wr_err<br>This bit indicates that during a DPI pixel line storage,the payload FIFO becomes full and the data stored is corrupted. |
| 6 | RO | 0x0 | eopt_err<br>This bit indicates that the EOTp packet is not received at the end of the incoming peripheral transmission. |
| 5 | RO | 0x0 | pkt_size_err<br>This bit indicates that the packet size error is detected during the packet reception. |
| 4 | RO | 0x0 | crc_err<br>This bit indicates that the CRC error is detected in a received packet. |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | ecc_multi_err<br>This bit indicates that the ECC multiple error is detected and corrected in a received packet. |
| 2 | RO | 0x0 | ecc_single_err<br>This bit indicates that the ECC single error is detected and corrected in a received packet. |
| 1 | RO | 0x0 | to_lp_rx<br>This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected. |
| 0 | RO | 0x0 | to_hs_tx<br>This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected. |

**MIPIC_MSK0**
Address: Operational Base + offset (0x00c4)
Masks the interrupt generation triggerd by the ERROR_ST0 reg

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x0 | reserved |
| 20 | RW | 0x0 | dphy_errors_4<br>This bit indicates LP1 contention error ErrContentionLP1 from Lane 0 |
| 19 | RW | 0x0 | dphy_errors_3<br>This bit indicates LP0 contention error ErrContentionLP0 from Lane 0 |
| 18 | RW | 0x0 | dphy_errors_2<br>This bit indicates control error ErrControl from Lane 0 |
| 17 | RW | 0x0 | dphy_errors_1<br>This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0 |
| 16 | RW | 0x0 | dphy_errors_0<br>This bit indicates ErrEsc escape entry error from Lane 0 |
| 15 | RW | 0x0 | ack_with_err_15<br>This bit retrieves the DSI protocol violation from the Display Acknowledge error report |
| 14 | RW | 0x0 | ack_with_err_14<br>This bit retrieves the reserved(specific to device) from the Display Acknowledge error report |
| 13 | RW | 0x0 | ack_with_err_13<br>This bit retrieves the invalid transmission length from the Display Acknowledge error report |
| 12 | RW | 0x0 | ack_with_err_12<br>This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report |

| Bit | Attr | Reset Value | Description |
| --- | --- | --- | --- |
| 11 | RW | 0x0 | ack_with_err_11<br>This bit retrieves the not recognized DSI data type from the Display Acknowledge error report |
| 10 | RW | 0x0 | ack_with_err_10<br>This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report |
| 9 | RW | 0x0 | ack_with_err_9<br>This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report |
| 8 | RW | 0x0 | ack_with_err_8<br>This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report |
| 7 | RW | 0x0 | ack_with_err_7<br>This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report |
| 6 | RW | 0x0 | ack_with_err_6<br>This bit retrieves the False Control error from the Display Acknowledge error report |
| 5 | RW | 0x0 | ack_with_err_5<br>This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report |
| 4 | RW | 0x0 | ack_with_err_4<br>This bit retrieves the LP Transmit Sync error error from the Display Acknowledge error report |
| 3 | RW | 0x0 | ack_with_err_3<br>This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report |
| 2 | RW | 0x0 | ack_with_err_2<br>This bit retrieves the EoT sync error from the Display Acknowledge error report |
| 1 | RW | 0x0 | ack_with_err_1<br>This bit retrieves the SoT Sync error from the Display Acknowledge error report |
| 0 | RW | 0x0 | ack_with_err_0<br>This bit retrieves the SoT error from the Display Acknowledge error report |

**MIPIC_MSK1**
Address: Operational Base + offset (0x00c8)
Masks the interrupt generation triggerd by the ERROR_ST1 reg

| Bit | Attr | Reset Value | Description |
| --- | --- | --- | --- |
| 31:13 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RO | 0x0 | gen_pld_recv_err<br>This bit indicates that during a generic interface packet read back,the payload FIFO becomes full and the received data is corrupted. |
| 11 | RO | 0x0 | gen_pld_rd_err<br>This bit indicates that during a DCS read data,the payload FIFO becomes empty and the data sent to the interface is corrupted |
| 10 | RO | 0x0 | gen_pld_send_err<br>This bit indicates that during a Generic interface packet build,the payload FIFO becomes empty and corrupt data is sent. |
| 9 | RO | 0x0 | gen_pld_wr_err<br>This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full.Therefore,the command is not written. |
| 8 | RO | 0x0 | gen_cmd_wr_err<br>This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full.Therefore,the command is not written. |
| 7 | RO | 0x0 | dpi_pld_wr_err<br>This bit indicates that during a DPI pixel line storage,the payload FIFO becomes full and the data stored is corrupted. |
| 6 | RO | 0x0 | eopt_err<br>This bit indicates that the EOTp packet is not received at the end of the incoming peripheral transmission. |
| 5 | RO | 0x0 | pkt_size_err<br>This bit indicates that the packet size error is detected during the packet reception. |
| 4 | RO | 0x0 | crc_err<br>This bit indicates that the CRC error is detected in a received packet. |
| 3 | RO | 0x0 | ecc_multi_err<br>This bit indicates that the ECC multiple error is detected and corrected in a received packet. |
| 2 | RO | 0x0 | ecc_single_err<br>This bit indicates that the ECC single error is detected and corrected in a received packet. |
| 1 | RO | 0x0 | to_lp_rx<br>This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected. |
| 0 | RO | 0x0 | to_hs_tx<br>This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected. |

## 45.5 Application Notes

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the Innosilicon D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

Perform the following steps to configure the DPI packet transmission:

Step1:Global configuration:
Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.

Step2:Configure the DPI Interface to define how the DPI interface interacts with the controller.
Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.
Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.
Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.
Configure vsync_active_low( DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
Configure vsync_active_low( DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
Configure vsync_active_low( DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.
Configure vsync_active_low( DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.
Configure en 18_loosely( DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.

Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.

Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.

Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DWC_mipi_dsi_host to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.
Configure the register fiedl vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size

(VID_PKT_CFG-[30:21]) are automatically ignored by the DWC_mipi_dsi_host.
Non-Burst mode: In this mode, the processor uses the partitioning properties of the DWC_mipi_dsi_host to divide the video line transmission into several DSI packets. This is done to match th pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration dose not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b0x.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b00x to enable the transmission of sync pulses.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b01to enable the transmission of sync events.
Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.
Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.
Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.
Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.
The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.
Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.
Step4:Define the DPI Horizontal timing configuration as follows:
Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DWC_mipi_dsi_host is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DWC_mipi_dsi_host can have a number of errors that can cause a malfunction of the video transmission.

Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).
Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.
Step5:Define the Vertical line configuration:
Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.
Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.
Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.
Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.