Chapter 31 SPI

31.1 Overview

The serial peripheral interface is an APB slave device. A fourwire fullduplex serial protocol from Motorola. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

31.1.1 Features

SPI Controllersupports the following features:

● Support Motorola SPI,TI Synchronous Serial Protocol and National Semiconductor Microwire interface
● Support 32-bit APB bus
● Support two internal 16-bit wide and 32-location deep FIFOs, one for transmitting and the other for receiving serial data
● Support two chip select signals in master mode
● Support 4,8,16 bit serial data transfer
● Support configurable interrupt polarity
● Support asynchronous APB bus and SPI clock
● Support master and slave mode
● Support DMA handshake interface and configurable DMA water level
● Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
● Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
● Support combine interrupt output
● Support up to half of SPI clock frequency transfer in master mode and one sixth of SPI clock frequency transfer in slave mode
● Support full and half duplex mode transfer
● Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
● Support configurable delay from chip select active to SCLK active in master mode
● Support configurable period of chip select inactive between two parallel data in master mode
● Support big and little endian, MSB and LSB first transfer
● Support two 8-bit audio data store together in one 16-bit wide location
● Support sample RXD 0~3 SPI clock cycles later
● Support configurable SCLK polarity and phase
● Support fix and incremental address access to transmit and receive FIFO

31.2 Block Diagram

The SPI Controller comprises with:

● AMBA APB interface and DMA Controller Interface
● Transmit and receive FIFO controllers and an FSM controller
● Register block
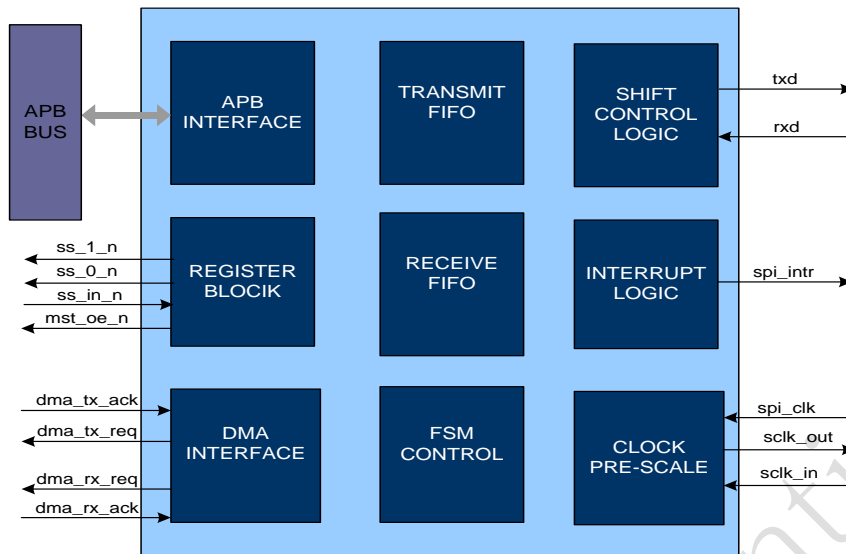
● Shift control and interrupt

Fig.31-1SPI Controller Block diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 8, 16, and 32 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serialdevice into the SPI is pushed into the receive FIFO. Both fifos are 32x16bits.

FSM CONTROL

Control the state's transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the AHB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit fifo or to the receive fifo. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can bemasked. The combined interrupt request is the ORed result of all other SPI interrupts after masking.
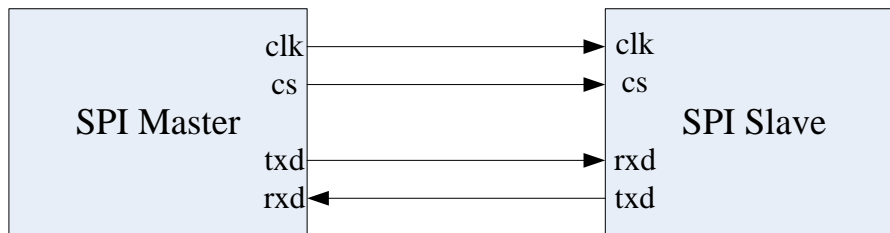
31.3 Function description

Fig.31-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram show how the SPI controller connects with other SPI devices.

Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1.

Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.

1. Transmit and Receive

When SPI_CTRLR0 [19:18]== 2'b00, both transmit and receive logic are valid.

2.Transmit Only

When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.

3.Receive Only

When SPI_CTRLR0 [19:18]== 2'b10, the transmit data are invalid.

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave,the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.
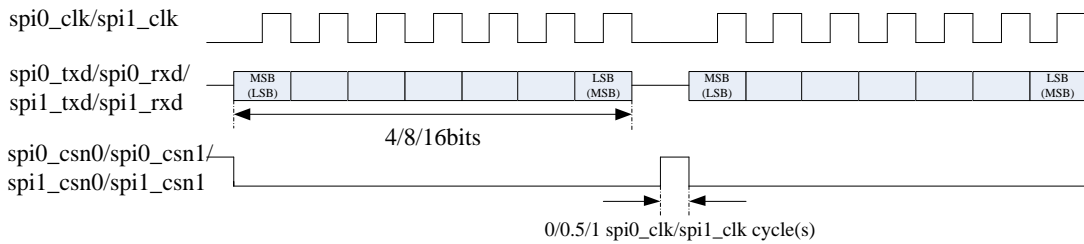
spi0_clk/spi1_clk

spi0_txd/spi0_rxd/
spi1_txd/spi1_rxd

spi0_csn0/spi0_csn1/
spi1_csn0/spi1_csn1

Fig.31-3SPI Format (SCPH=0 SCPOL=0)

spi0_clk/spi1_clk

spi0_txd/spi0_rxd/
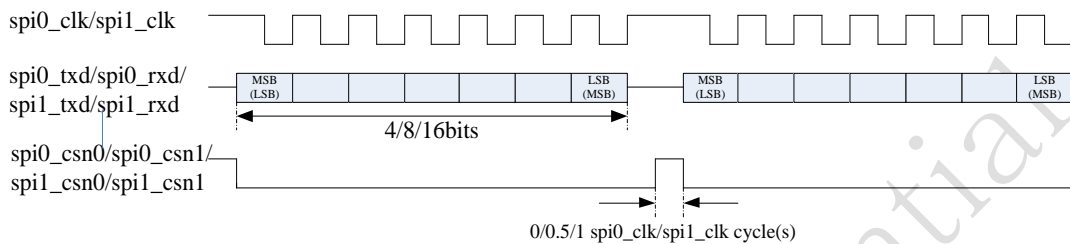spi1_txd/spi1_rxd

spi0_csn0/spi0_csn1/
spi1_csn0/spi1_csn1

Fig.31-4SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

spi0_clk/spi1_clk

spi0_txd/spi0_rxd/
spi1_txd/spi1_rxd

spi0_csn0/spi0_csn1/
spi1_csn0/spi1_csn1

Fig.31-5SPI Format (SCPH=1 SCPOL=0)

spi0_clk/spi1_clk
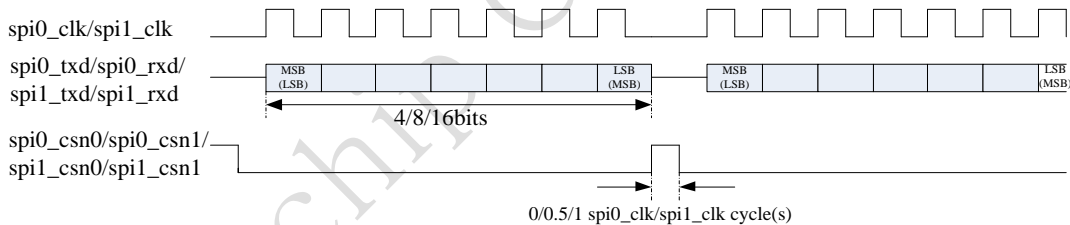
spi0_txd/spi0_rxd/
spi1_txd/spi1_rxd

spi0_csn0/spi0_csn1/
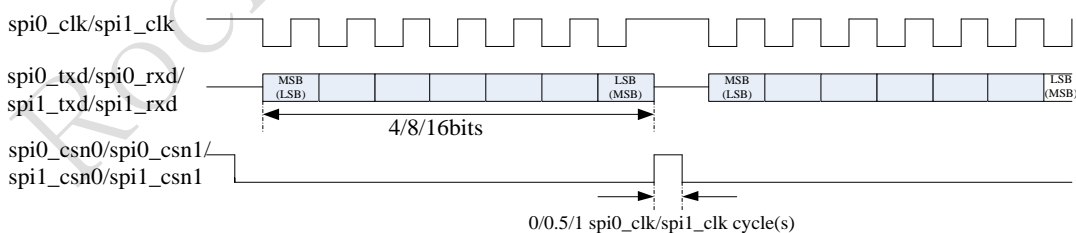spi1_csn0/spi1_csn1

Fig.31-6SPI Format (SCPH=1 SCPOL=1)

31.4 Register Description

This section describes the control/status registers of the design. Pay attention that there are two SPI controllers in the chip: spi0 & spi1, so the base address in the following register descriptions can be either spi0 or spi1 base address.

31.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00000002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable
SPI_SER	0x000c	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001c	W	0x00000000	Transmit FIFO Level
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level
SPI_SR	0x0024	W	0x0000000c	SPI Status
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity
SPI_IMR	0x002c	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003c	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_TXDR	0x0400~0x07fc	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800~0x0bfc	W	0x00000000	Receive FIFO Data

Notes:<u>Size:</u>**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

31.4.2 Detail Register Description

SPI_CTRLR0
Address: Operational Base + offset (0x0000)
Control Register 0

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	MTM Microwire Transfer Mode Valid when frame format is set to National Semiconductors Microwire. 1'b0: non-sequential transfer 1'b1: sequential transfer
20	RW	0x0	OPM Operation Mode 1'b0: Master Mode 1'b1: Slave Mode

Bit	Attr	Reset Value	Description
19:18	RW	0x0	XFM Transfer Mode 2'b00 :Transmit & Receive 2'b01 : Transmit Only 2'b10 : Receive Only 2'b11 :reserved
17:16	RW	0x0	FRF Frame Format 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11 : Reserved
15:14	RW	0x0	RSD Rxd Sample Delay When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00:do not delay 2'b01:1 cycle delay 2'b10:2 cycles delay 2'b11:3 cycles delay
13	RW	0x0	BHT Byte and Halfword Transform Valid when data frame size is 8bit. 1'b0:apb 16bit write/read, spi 8bit write/read 1'b1: apb 8bit write/read, spi 8bit write/read
12	RW	0x0	FBM First Bit Mode 1'b0:first bit is MSB 1'b1:first bit is LSB
11	RW	0x0	EM Endian Mode Serial endian mode can be configured by this bit. Apb endian mode is always little endian. 1'b0:little endian 1'b1:big endian
10	RW	0x0	SSD ss_n to sclk_out delay Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: the period between ss_n active and sclk_out active is half sclk_out cycles. 1'b1: the period between ss_n active and sclk_out active is one sclk_out cycle.

Bit	Attr	Reset Value	Description
9:8	RW	0x0	CSM Chip Select Mode Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred. 2'b01:ss_n be high for half sclk_out cycles after every frame data is transferred. 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred. 2'b11:reserved
7	RW	0x0	SCPOL Serial Clock Polarity Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low 1'b1: Inactive state of serial clock is high
6	RW	0x0	SCPH Serial Clock Phase Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit 1'b1: Serial clock toggles at start of first data bit
5:2	RW	0x0	CFS Control Frame Size Selects the length of the control word for the Microwire frame format. 4'b0000~4'b0010:reserved 4'b0011:4-bit serial data transfer 4'b0100:5-bit serial data transfer 4'b0101:6-bit serial data transfer 4'b0110:7-bit serial data transfer 4'b0111:8-bit serial data transfer 4'b1000:9-bit serial data transfer 4'b1001:10-bit serial data transfer 4'b1010:11-bit serial data transfer 4'b1011:12-bit serial data transfer 4'b1100:13-bit serial data transfer 4'b1101:14-bit serial data transfer 4'b1110:15-bit serial data transfer 4'b1111:16-bit serial data transfer
1:0	RW	0x2	DFS Data Frame Size Selects the data frame length. 2'b00:4bit data 2'b01:8bit data 2'b10:16bit data 2'b11:reserved

SPI_CTRLR1

Address: Operational Base + offset (0x0004)
Control Register 1

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	NDM Number of Data Frames When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer.

SPI_ENR
Address: Operational Base + offset (0x0008)
SPI Enable

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	ENR SPI Enable Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER
Address: Operational Base + offset (0x000c)
Slave Enable Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	SER Slave Select Enable This register is valid only when SPI is configured as a master device.

SPI_BAUDR
Address: Operational Base + offset (0x0010)
Baud Rate Select

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BAUDR Baud Rate Select SPI Clock Divider. This register is valid only when the SPI is configured as a master device. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/ SCKDV Where SCKDV is any even value between 2 and 65534. For example: for Fspi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR
Address: Operational Base + offset (0x0014)
Transmit FIFO Threshold Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	TXFTLR Transmit FIFO Threshold Level When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR
Address: Operational Base + offset (0x0018)
Receive FIFO Threshold Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	RXFTLR Receive FIFO Threshold Level When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR
Address: Operational Base + offset (0x001c)
Transmit FIFO Level

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RO	0x00	TXFLR Transmit FIFO Level Contains the number of valid data entries in the transmit FIFO.

SPI_RXFLR
Address: Operational Base + offset (0x0020)
Receive FIFO Level

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RO	0x00	RXFLR Receive FIFO Level Contains the number of valid data entries in the receive FIFO.

SPI_SR
Address: Operational Base + offset (0x0024)
SPI Status

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	RFF Receive FIFO Full 1'b0: Receive FIFO is not full 1'b1: Receive FIFO is full
3	RO	0x1	RFE Receive FIFO Empty 1'b0: Receive FIFO is not empty 1'b1: Receive FIFO is empty
2	RO	0x1	TFE Transmit FIFO Empty 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty
1	RO	0x0	TFF Transmit FIFO Full 1'b0: Transmit FIFO is not full 1'b1: Transmit FIFO is full
0	RO	0x0	BSF SPI Busy Flag When set, indicates that a serial transfer is in progress; when cleared indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled 1'b1: SPI is actively transferring data

SPI_IPR
Address: Operational Base + offset (0x0028)
Interrupt Polarity

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	IPR Interrupt Polarity Interrupt Polarity Register 1'b0:Active Interrupt Polarity Level is HIGH 1'b1: Active Interrupt Polarity Level is LOW

SPI_IMR
Address: Operational Base + offset (0x002c)
Interrupt Mask

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	RFFIM Receive FIFO Full Interrupt Mask 1'b0: spi_rxf_intr interrupt is masked 1'b1: spi_rxf_intr interrupt is not masked
3	RW	0x0	RFOIM Receive FIFO Overflow Interrupt Mask 1'b0: spi_rxo_intr interrupt is masked 1'b1: spi_rxo_intr interrupt is not masked
2	RW	0x0	RFUIM Receive FIFO Underflow Interrupt Mask 1'b0: spi_rxu_intr interrupt is masked 1'b1: spi_rxu_intr interrupt is not masked
1	RW	0x0	TFOIM Transmit FIFO Overflow Interrupt Mask 1'b0: spi_txo_intr interrupt is masked 1'b1: spi_txo_intr interrupt is not masked
0	RW	0x0	TFEIM Transmit FIFO Empty Interrupt Mask 1'b0: spi_txe_intr interrupt is masked 1'b1: spi_txe_intr interrupt is not masked

SPI_ISR
Address: Operational Base + offset (0x0030)
Interrupt Status

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	RFFIS Receive FIFO Full Interrupt Status 1'b0: spi_rxf_intr interrupt is not active after masking 1'b1: spi_rxf_intr interrupt is full after masking
3	RO	0x0	RFOIS Receive FIFO Overflow Interrupt Status 1'b0: spi_rxo_intr interrupt is not active after masking 1'b1: spi_rxo_intr interrupt is active after masking

Bit	Attr	Reset Value	Description
2	RO	0x0	RFUIS Receive FIFO Underflow Interrupt Status 1'b0: spi_rxu_intr interrupt is not active after masking 1'b1: spi_rxu_intr interrupt is active after masking
1	RO	0x0	TFOIS Transmit FIFO Overflow Interrupt Status 1'b0: spi_txo_intr interrupt is not active after masking 1'b1: spi_txo_intr interrupt is active after masking
0	RO	0x0	TFEIS Transmit FIFO Empty Interrupt Status 1'b0: spi_txe_intr interrupt is not active after masking 1'b1: spi_txe_intr interrupt is active after masking

SPI_RISR
Address: Operational Base + offset (0x0034)
Raw Interrupt Status

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	RFFRIS Receive FIFO Full Raw Interrupt Status 1'b0: spi_rxf_intr interrupt is not active prior to masking 1'b1: spi_rxf_intr interrupt is full prior to masking
3	RO	0x0	RFORIS Receive FIFO Overflow Raw Interrupt Status 1'b0:spi_rxo_intr interrupt is not active prior to masking 1'b1:spi_rxo_intr interrupt is active prior to masking
2	RO	0x0	RFURIS Receive FIFO Underflow Raw Interrupt Status 1'b0: spi_rxu_intr interrupt is not active prior to masking 1'b1: spi_rxu_intr interrupt is active prior to masking
1	RO	0x0	TFORIS Transmit FIFO Overflow Raw Interrupt Status 1'b0: spi_txo_intr interrupt is not active prior to masking 1'b1: spi_txo_intr interrupt is active prior to masking

Bit	Attr	Reset Value	Description
0	RO	0x1	TFERIS Transmit FIFO Empty Raw Interrupt Status 1'b0: spi_txe_intr interrupt is not active prior to masking 1'b1: spi_txe_intr interrupt is active prior to masking

SPI_ICR
Address: Operational Base + offset (0x0038)
Interrupt Clear

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	WO	0x0	CTFOI Clear Transmit FIFO Overflow Interrupt Write 1 to Clear Transmit FIFO Overflow Interrupt
2	WO	0x0	CRFOI Clear Receive FIFO Overflow Interrupt Write 1 to Clear Receive FIFO Overflow Interrupt
1	WO	0x0	CRFUI Clear Receive FIFO Underflow Interrupt Write 1 to Clear Receive FIFO Underflow Interrupt
0	WO	0x0	CCI Clear Combined Interrupt Write 1 to Clear Combined Interrupt

SPI_DMACR
Address: Operational Base + offset (0x003c)
DMA Control

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	TDE Transmit DMA Enable 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
0	RW	0x0	RDE Receive DMA Enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled

SPI_DMATDLR
Address: Operational Base + offset (0x0040)
DMA Transmit Data Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and Transmit DMA Enable (DMACR[1]) = 1.

SPI_DMARDLR
Address: Operational Base + offset (0x0044)
DMA Receive Data Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	RDL Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and Receive DMA Enable(DMACR[0])=1.

SPI_TXDR
Address: Operational Base + offset (0x0400~0x07fc)
Transmit FIFO Data

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	WO	0x0000	TXDR Transimt FIFO Data Register. When it is written to, data are moved into the transmit FIFO.

SPI_RXDR
Address: Operational Base + offset (0x0800~0x0bfc)
Receive FIFO Data

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	RXDR Receive FIFO Data Register. When the register is read, data in the receive FIFO is accessed.

31.5 Interface description

SPI have 3 IOMUX, which is controlled by GRF_SOC_CON1[4:3].
When GRF_SOC_CON1[4:3] is 2'b00. The IOMUX is as follow.

Table 31-1SPI interface description in master mode

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_SPIclk_UART1ctsn_GPIO1b0	GRF_GPIO1B_IOMUX[1:0]=2'b01
spi_csn0	I/O	IO_SPIcsn0_UART1rtsn_GPIO1b3	GRF_GPIO1B_IOMUX[7:6]=2'b01
spi_txd	O	IO_SPItxd_UART1sout_GPIO1b1	GRF_GPIO1B_IOMUX[3:2]=2'b01
spi_rxd	I	IO_SPIrxd_UART1sin_GPIO1b2	GRF_GPIO1B_IOMUX[5:4]=2'b01
spi_csn1	O	IO_SPIcsn1_GPIO1b4	GRF_GPIO1B_IOMUX[8]=1'b1

Note: spi0_csn1, spi1_csn1 can only be used in master mode

Table 31-2SPI interface description in slave mode

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_SPIclk_UART1ctsn_GPIO1b0	GRF_GPIO1B_IOMUX[1:0]=2'b01
spi_csn0	I/O	IO_SPIcsn0_UART1rtsn_GPIO1b3	GRF_GPIO1B_IOMUX[7:6]=2'b01
spi_txd	O	IO_SPItxd_UART1sout_GPIO1b1	GRF_GPIO1B_IOMUX[3:2]=2'b01
spi_rxd	I	IO_SPIrxd_UART1sin_GPIO1b2	GRF_GPIO1B_IOMUX[5:4]=2'b01

When GRF_SOC_CON1[4:3] is 2'b01. The IOMUX is as follow.

Table 31-3 SPI interface description in master mode

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_NANDale_SPI1clk_GPIO2a0	GRF_GPIO2A_IOMUX[1:0]=2'b10
spi_csn0	I/O	IO_NANDd6_EMMCd6_SPI1csn0_GPIO1d6	GRF_GPIO1D_IOMUX[13:12]=2'b11
spi_txd	O	IO_NANDd5_EMMCd5_SPI1txd1_GPIO1d5	GRF_GPIO1D_IOMUX[11:10]=2'b11
spi_rxd	I	IO_NANDd4_EMMCd4_SPI1rxd1_GPIO1d4	GRF_GPIO1D_IOMUX[9:8]=2'b11
spi_csn1	O	IO_NANDd7_EMMCd7_SPI1csn1_GPIO1d7	GRF_GPIO1D_IOMUX[15:14]=2'b11

Note: spi0_csn1, spi1_csn1 can only be used in master mode

Table 31-4 SPI interface description in slave mode

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_NANDale _SPI1clk_GP IO2a0	GRF_GPIO2A_IOMUX[1:0]=2'b10
spi_csn0	I/O	IO_NANDd6 _EMMCd6_S PI1csn0_GP IO1d6	GRF_GPIO1D_IOMUX[13:12]=2'b11
spi_txd	O	IO_NANDd5 _EMMCd5_S PI1txd1_GPI O1d5	GRF_GPIO1D_IOMUX[11:10]=2'b11
spi_rxd	I	IO_NANDd4 _EMMCd4_S PI1rxd1_GPI O1d4	GRF_GPIO1D_IOMUX[9:8]=2'b11

When GRF_SOC_CON1[4:3] is 2'b10. The IOMUX is as follow.

Table 31-5 SPI interface description in master mode

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_I2S1sclk_SP Iclkm_GPIO0b1	GRF_GPIO0B_IOMUX[3:2]=2'b10
spi_csn0	I/O	IO_I2S1sdi_SPI csn0m_GPIO0b6	GRF_GPIO0B_IOMUX[13:12]=2'b10
spi_txd	O	IO_I2S1lrckrx_S PItxdm_GPIO0b 3	GRF_GPIO0B_IOMUX[7:6]=2'b10
spi_rxd	I	IO_I2S1sdo_SPI rxdm_GPIO0b5	GRF_GPIO0B_IOMUX[11:10]=2'b10

Table 31-6 SPI interface description in slave mode

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_I2S1sclk _SPIclkm_G PIO0b1	GRF_GPIO0B_IOMUX[3:2]=2'b10
spi_csn0	I/O	IO_I2S1sdi_ SPIcsn0m_G PIO0b6	GRF_GPIO0B_IOMUX[13:12]=2'b10
spi_txd	O	IO_I2S1lrck rx_SPItxdm _GPIO0b3	GRF_GPIO0B_IOMUX[7:6]=2'b10
spi_rxd	I	IO_I2S1sdo _SPIrxdm_G PIO0b5	GRF_GPIO0B_IOMUX[11:10]=2'b10

31.6 Application Notes

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock

(sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,

When SPI Controller works as master, theF_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave,the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.
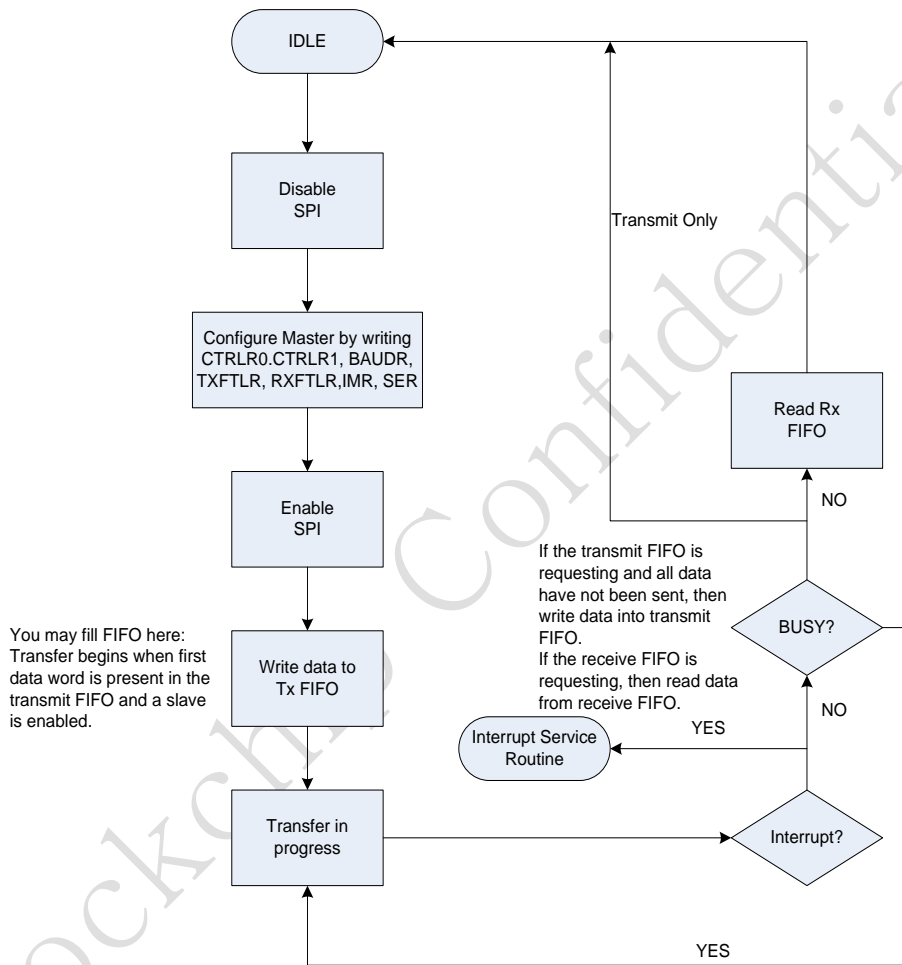

Fig.31-7SPI Master transfer flow diagram

Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its txd data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.
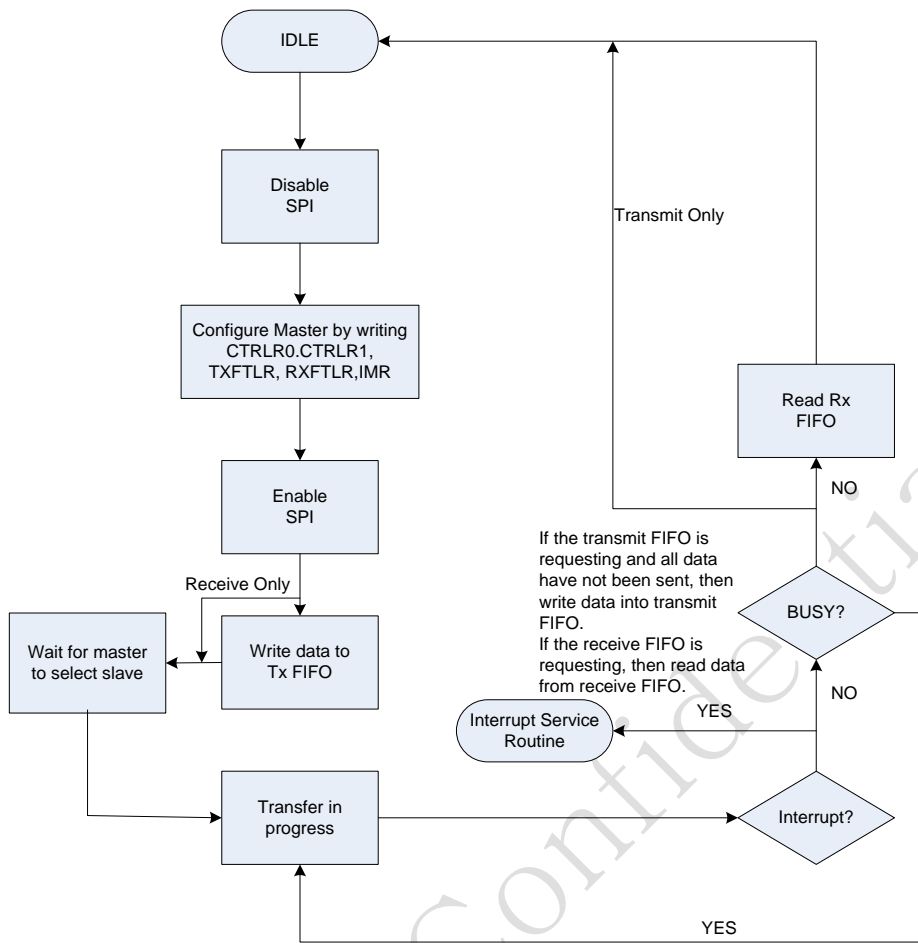
Fig.31-8SPI Slave transfer flow diagram