Chapter 31 Image Signal Processing (ISP)

31.1 Overview

The Image Signal Processing (ISP) represents a complete video and still picture input unit. It contains image processing, scaling, and compression functions. The integrated image processing unit supports simple CMOS sensors delivering RGB Bayer pattern without any integrated image processing and also image sensors with integrated YCbCr processing.

Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data stream for MPEG-4 compression. In general, YCbCr 4:2:2 JPEG compressed images should use the full sensor resolution, but they can also be downscaled to a lower resolution for smaller JPEG files. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.

An image effects block is present which can create images with sepia, black&white, color selection, negative, emboss and sketch effects.

The camera interface provides SMIA and/or MIPI support, so that ISP can be connected to PHY devices or IP blocks directly.

All data is transmitted via the memory interface to a BVCI/AXI bus system using a bus master interface.

Programming is done by register read/write transactions using an PVCI slave interface.

ISP supports the following features:

- Generic Sensor Interface with programmable polarity for synchronization signals
- ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
- 12 bit camera interface
- 12 bit resolution per color component internally
- YCbCr 4:2:2 processing
- Flash light control
- Mechanical shutter support
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
- Windowing and frame synchronization
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Continuous resize support
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data and JPEG files
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue, offset, range)
- Power management by software controlled clock disabling of currently not needed sub-modules
- Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
- Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
- Read port provided to read back a picture from system memory
- Simultaneous picture read back, resizing and storing through self path while main path captures the camera picture

- Black level compensation
- Four channel Lens shade correction (Vignetting)
- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Global Tone Mapping with wide dynamic range unit (WDR)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction
- AXI 64 bit interface 32Bit Address range (two DMA-write ports and one DMA-read port)
- Up to 16 Beat Bursts depending on configured FIFO size
- 32 bit AHB programming interface
- Maximum input resolution of 4416x3312 pixels
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
- Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
- Support of semiplanar NV21 color storage format
- Support of independent image cropping on main and self path

31.2 Block Diagram

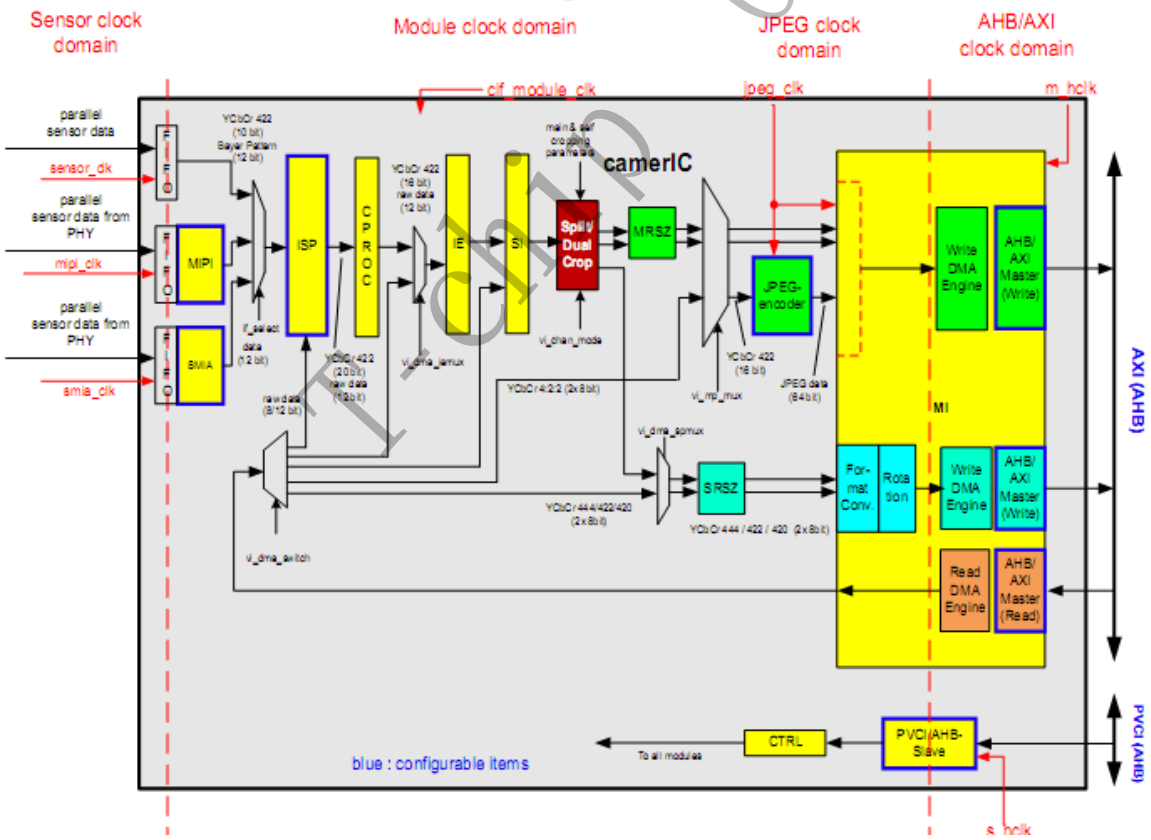

Fig. 31-1 ISP Block Diagram

ISP comprises with:

- MIPI serial camera interface
- Image Signal Processing (ISP)
- Color Processing (CPROC)
- Image Effects (IE)
- Superimpose (SI)
- Luminance /Chrominance Splitter (Y/C Split)
- Main and Self Crop (Dual Crop)
- Main Resize (MRSZ)
- JPEG Encoder
- MPMUX for selection of main path data flow
- SPMUX for selection of self-scaler input data
- Self Resize (SRSZ)
- Memory Interface (MI) including YCbCr to RGB conversion for self-picture and image rotation
- Control Unit

31.3 Function Description

31.3.1 MIPI

The MIPI interface is the second optional serial camera interface of ISP Controller. The interface is implemented according to the CSI2 specification defined by the MIPI Alliance, connecting a PPI data interface to a MIPI_D-PHY physical layer with a 12bits ALOMICs interface.

Features and Standard Compliance

Compliant to MIPI Alliance Standard for Camera Serial Interface 2 (CSI2)

- PPI Interface according to D-PHY specification, Annex A
- Supports up to 4 data lanes (extendable by request)
- Number of lanes is programmable and hardware configurable
- Provides lane merging, error detection and correction, virtual channel detection, programmable data extraction and embedded data separation
- Supported data types are:
  - Generic 8bit data
  - Non-legacy YUV 4:2:0 8bit / 10bit with cosited chroma sampling
  - Non-legacy YUV 4:2:0 8bit / 10bit with non-cosited chroma sampling
  - Legacy YUV 4:2:0 8bit
  - YUV 4:2:2 8bit / 10bit
  - RGB 444 / 555 / 565 / 666 / 888 image data
  - RAW 6-bit / 7-bit / 8-bit / 10-bit / 12-bit image data
  - User-defined 8-bit data
- PVCI similar output interface
- PVCI control interface

RAW 14-bit image data types are not supported. The MIPI D-PHY-Layer features Escape Modus and Low Power Data Transfer are not needed for the Protocol Receiver. According to the CSI2 specification only unidirectional high-speed data transfer is mandatory for the camera interface.

31.3.2 ISP Block

The ISP block includes the interface to the attached parallel sensor device and the MIPI interfaces. It accepts either ITU-R BT 601 YCbCr, well as raw Bayer data or ITU-R BT 656 YCbCr data. The order of Y and Cx as well as Cb and Cr is programmable. It contains the interpolation filter for the raw Bayer to plain RGB conversion.

An input acquisition window is programmable supporting detection of smaller than programmed input images. An error IRQ is generated in case of input error conditions.

The ISP allows programming of a continuous image sampling mode, or a mode where the number of images to be sampled subsequently can be programmed (1…1023).

Additionally it incorporates image quality improvements (gamma correction, black level subtraction, white balancing, etc.).

The ISP block supports also auto exposure capabilities by providing image color statistics information to the system processor for correct sensor device programming.

The input part of the ISP block is fully programmable in terms of signal polarities, active video data positions, and luminance/chrominance order.

The ISP block always delivers YCbCr 4:2:2 data at its output port. Data provided by the RGB channel are downsampled to YCbCr 4:2:2, supporting both co-sited and non co-sited calculation. Luminance and chrominance data are provided in parallel using line and frame end signals. In raw data mode (unprocessed data) these data are transferred via the Y port.

Handshaking is used for data qualification. As the sensor device cannot be stopped delivering data the backward handshake (acknowledge) is only used for pixel drop detection which is signaled using an IRQ. To prevent pixel dropping a latency FIFO is implemented. The FIFO depth can be option of customization.

The ISP block also contains its own programming registers to be accessed by a 32 bit PVCI compliant interface supporting single transfers only.

The incoming hsync and vsync control signals from the camera are connected to interrupt logic. It is possible to trigger on these signals for an event triggered configuration during processing.

DPCC

The ISP core is designed to operate with high-end, mid-range and low-end image sensors, which mainly differ in the number of pixels and module cost. While high-end sensors aim at a high number of pixels with sufficiently large pixel area, low-cost modules often have a large number of defects. Additionally, for low cost sensors in the manufacturing process no time is available for determining the defect pixels locations.

Another problem is that hot pixels get visible at long integration times and can get a high density up to 5%. This means 250000 defect pixels for a 5 Megapixel sensor.

An improved algorithm has been developed, named Defect Pixel Cluster Correction (DPCC). This is an on-the-fly detection and replacement processing as well as a table based replacement method

Defect Pixel Detection

For each pixel threshold values are calculated by several methods, using the correlation of neighbor pixel of the same color (red, green or blue) with exception of the peak gradient estimation for red and blue that also uses the green pixel values in the 5x5 neighborhood of the raw Bayer image. These methods use statistical properties and linear prediction to determine if a pixel needs to be marked as defect. A 3x3 sorting algorithm with rank estimation including the calculation of median values of some pixel groups is a central unit. Output of the detection unit is a marker signal for the following correction stage to indicate, if the current pixel is defect. The detection can be controlled by programmable threshold values, factors and options which methods should be used. The correct setting of the thresholds is important for a good separation between defects and keeping high resolution and detail features in the image.

Defect Pixel Table control

A defect pixel table is implemented as SRAM of user defined size containing entries with defect

pixel coordinates. The table control generates a replace flag independently from the on-the-fly detection, so that table correction and on-the-fly correction can be operated in parallel.

Defect Pixel Replacement

Basic algorithm is a switching median filter, which performs sorting and rank ordering. The replacement unit takes the information of the Defect Pixel Detection as input. It uses a statistical sorting filter (median filter) separately for each color to determine the nearest neighbor value for replacement. The filter size is 4 (upper, lower, left and right neighbor for red/blue or diagonal neighbors for green) optionally 5, including the center pixel. The condition for successfull replacement is that NOT more than 4 of 9 pixels are defect. So correction of single and small cluster defects of 1x3 (3x1) and 2x2 pixels is possible (please note these clusters belong to a single color in the bayer pattern).

9. Auto Focus Measurement

An auto-focus measurement block is implemented to support auto-focus control. A substantial part of auto-focus control will be done software supported: The search algorithm which looks for maximum sharpness in the image is implemented using software and the movement of the lens is controlled by software. The auto-focus module which is implemented using hardware delivers measurement values of image sharpness via a register interface.

The module measures the sharpness in 3 windows of selectable size via register settings. The auto-focus measurement block uses the line buffer of the emosaicing block. The data in the buffer are stored in Bayer format and read 3-line-wise (top, middle, bottom).

10. Filter (Noise Reduction, Sharpness, Blurring)

As mentioned above, high-end, mid-range and low-end image sensors mainly differ in the number of pixels and module cost. While high end sensors aim at a high number of pixels with sufficiently large pixel area, low-cost modules have small pixels and lens with small diameter. This combination of small lens diameter and small pixels results in higher pixel noise at a given level of illumination than in high end sensors.

To improve the visual image quality, noise and artifacts of the Bayer Matrix should be eliminated and sharpness should be increased. These are requirements which cannot be easily combined.

Noise and the artifacts of the Bayer pattern must be eliminated by averaging or blurring filters. Sharpness could be improved by a high pass or Laplace filter.

Texture detection allows detecting planes or edges, high or low density of details.

With this texture information an adaptive filter is controlled which reduces noise in planes and improves sharpness in detailed regions. If there are less details below or near the noise level two-dimensional blurring is applied. With a higher detail level, the blurring is done along detected edges or lines. If improvement of sharpness is required, the sharpness will be enhanced orthogonally to the direction of the blurring operation.

For example if a horizontal edge is detected, blurring will be done in horizontal direction and sharpness will be improved in vertical direction. In regions with highest contrast and details the filter can be bypassed or if sharpness improvement is required, a two dimensional sharpness filter is realized.

Additionally if no noise reduction is required a fixed blurring or sharpness filter can be selected. The sharpness can be improved by a fixed sharpness filter or edge depending as described beyond.

The noise reduction level can be adapted by the filter coefficients which determine the weightiness of averaging, and by the threshold values which are compared with the texture detection results.

For an optimal noise reduction it is important to know the effective noise level. If the noise

level is too high, the noise cannot be eliminated at the best possible rate. If the noise level is low and the noise reduction level is too high, too much details of the image will be lost unnecessarily.

If the light conditions are known, the noise level can be estimated using a table from the exposure settings of the image sensor. If the noise level must be calculated e.g. from the variance of the image RGB data, it is difficult to decide if the variance is caused by the noise or by image patterns.

In addition the hardware effort for separate filters is high because of the necessary line buffers. Therefore the filter algorithm is combined with demosaicing, so that the same line buffer can be used for demosaicing, noise filtering and blurring/sharpening.

The combined demosaicing filter module is designed to operate with linear RGB white balanced Bayer Data. So for best results of interpolation for demosaicing and of texture detection the RGB data should be optimal white balanced.

11. Video Stabilization

The ISP Controller Video Stabilization consists of the following components

- Video Stabilization Measurement
- Video Stabilization Software
- ISP Image Stabililzer

The Video Stabilization Measurement is done in hardware. It calculates per image the horizontal and vertical displacement vector for global motion in comparison to the previous image.

The Video Stabilization Software reads these measurements values, applies some smoothing algorithms and provides the respective cropping window to the ISP Image Stabilization.

The ISP Image Stabilization crops the image with respect to the given cropping window.

The cropping of an image has to be done after the video stabilization measurement for the image has been completed. This involves the usage of at least 1 frame buffer in system memory.

The Image Stabilizer unit delivers YUV data (either unmodified YUV data received as ITU-R BT.601 or ITU-R BT.656 data or color-processed image data) to the following ISP Controller environment.

The Video Stabilization process is currently limited to input line sizes of 2048 pixels and output line sizes of 1280 pixels.

12. Mechanical Shutter Control

With increasing sensor resolution the expectation of high quality pictures also rises. Therefore the exposure control must be decoupled from the frame rate and data read-out. This can be achieved by a mechanical shutter. The mechanical shutter control supports shutter speeds from 1/4000 sec to 10.7 sec by 48-100MHz.

13. Flash Light Control

The sensor interface supports triggering of a LED or tube flash light. The flash light output and the prelight output can be used to control a flash light device. Both the flash light and the prelight are activated by a trigger event. This event may either be a positive or negative edge from the camera or a positive edge from any other trigger source at the input port 'vds_vsync'.

Signal polarity, flash delay time and flash light time are determined by programming respective configuration register.

14. Histogram Calculation

A histogram function is implemented which counts the number of pixels with the same value. In general this histogram is a graphical representation of the pattern of variation that exists in the intensity values of the color or luminance planes.

Usually it is displayed by vertical bars drawn to indicate frequency levels of data collected within specific ranges. This measurement block can be used for different purposes. The most obvious application is an informative display for the end user. It is used for improving the exposure control, which is done by a software control loop.

Histogram Calculation is done independently for 5x5 windows which is important for advanced and fast auto exposure algorithms with complex scene detection.

15. Lens Shading Correction

The lens shading correction deals with the problems of vignetting and lens shading. It is done during input data processing: If the lens shading correction is enabled, each pixel is processed and corrected according to the stored settings. The lens shading correction is done by multiplying each input pixel with its respective correction value.

Only the correction factors at predefined sector corners as well as the sector positions are stored. The pixel position specific correction values are calculated using bilinear interpolation.

The correction factors at the sector corners are calculated during a calibration process which uses one or more reference frames which have to be captured under dedicated light conditions and at a dedicated position of the sensor. The captured frames are evaluated by software and the calculated parameters for lens shading correction are stored in multiple illumination specific tables e.g. in external memory or on a flash device. The software controls the lens shading process by loading or updating the correct tables into the hardware module.

It is also possible to use different lens shading correction parameters for different environment conditions, e.g. lightness, light direction or sensor position.

16. Wide Dynamic Range (WDR)

ISP contains a global tone and color mapping unit for Wide Dynamic Range (WDR) compression. Compared with a standard camera, the dynamic range of input intensities appears to be widened, since more structure becomes visible out of the dark and bright image regions.

The dynamic range of real-word scenes is much higher than the available dynamic range of low cost CMOS image sensors. The image sensor thus captures a small range of the real word's scene radiance and maps it to the available output range of the sensor. Radiance levels above or below the sensor's value range are clipped to black or white in the sensor.

The auto-exposure control (AEC) controls which portion of the scene radiance is mapped to the sensor value range. The AEC uses a model-driven scene evaluation to determine the best exposure value.

Nevertheless, there is a chance that portions in the scene are mapped to the dark grey tones or near white tones. This is the case especially in high contrast scenes, when there is anyhow not the chance to perfectly reproduce the full scene radiance range.

Global tone mapping can be used to reduce this effect. It aims at shifting textures in dark grey or near white tones into the mid tone range and thus allows to optimize the perceptual reproduction of the scene. Compared with a standard camera, the dynamic range of input intensities appears to be widened, since more structure becomes visible out of the dark and bright image regions.

This step is being performed directly before the Gamma-Correction. Basically by applying a scene dependent tone curve the required intensity shift is being performed.

During this step the following constraints have to be considered:

- Shifting of textures from dark grey into mid tones increases noise. Thus this step should only be performed for images with a sufficiently low noise level in dark grey tones.
- Changing the intensity level of a pixel also effects the color saturation. In order to avoid color clipping a correction of the color saturation is to be performed. This ensures that after tone mapping the colors have the same hue as before.

The tone and color clipping correction unit for wide dynamic range applications (WDR) for MARVIN performs scene dependent correction such as brightening of dark texture tones. Suitably, the MARVIN denoising pre-filter is being used for edge-preserving noise reduction especially in dark textures. Additionally, color clipping compensation is being performed with tone mapping.

31.3.3 Color Processing

The Color Processing block is responsible for color processing functions, i.e. hue, contrast, brightness, and saturation adjustment. It operates at YCbCr 4:2:2 data.

31.3.4 Image Effects (IE)

The Image Effects block modifies an image by pixel modifications. A set of different modifications can be applied: grayscale-, sepia-, color selection-, negative-, emboss-, sketch and sharpening effects

In addition a solarize effect can be created by using the gamma block of ISP Controller (for more information an application note is available).

The Image Effects module gets YCbCr 4:2:2 data via a 16 bit ([15:8]: Y, [7:0]: Cb/Cr) data interface.

IE Feature

- Data input- and output handshake interface
- Supports YCbCr 4:2:2 format
- 3x3 Laplace Filter (for picture edge extraction used for emboss, sketch and sharpening effects)
- ITU-R BT.601 compliant YCbCr to RGB conversion (used for the color selection effect to compare red green blue components of a pixel with defined threshold values)

31.3.5 Super Impose (SI)

The Super Impose module overlays an image with a bitmap from the main memory

- Color of the transparent area in superimpose bitmap is configurable. So the camera picture interfuses through the transparent area (A).
- Furthermore the Superimpose block is able to position a bitmap with the appropriate coordinates over the camera image range (B).

The Super Impose module gets picture data in YCbCr 4:2:2 formats via a 16 bit data interface from the Image Effects module. The Memory Interface module delivers the Y, Cb and Cr pixel components of the superimpose bitmap through three independent handshake data interfaces. Within the common area of the two pictures, output pixel data is determined by the bitmap from main memory or by the image from the Image Effects module.

31.3.6 Luminance/Chrominance Splitter (YC_Split)

The Luminance / Chrominance Splitter is responsible for providing component separated YCbCr 4:2:2 pixel data for further processing. Therefore it has to split the data path for chrominance and luminance values as well as for main and self-picture path.

31.3.7 Resize (Main and Self Scaler)

The Resize module is instantiated twice in ISP Controller: One instance for the main path (main resize, MRSZ) and one for the self path (self resize, SRSZ). The Resize Modules get pictures in YCbCr 4:2:2 format, and scale them by an arbitrary factor up or down to a new format. See following Figure for a module overview:

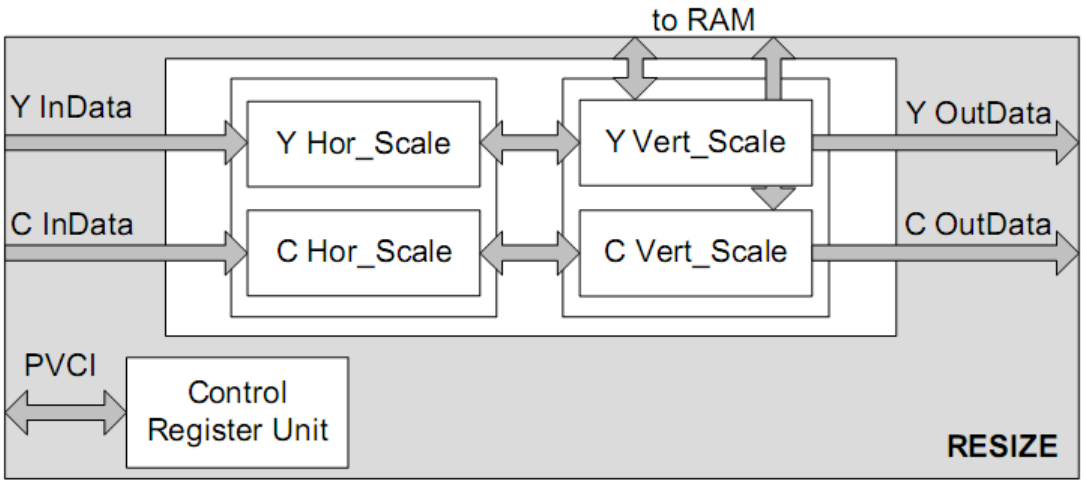

Fig. 31-2 Block Diagram of the Resize Module

Feature and Standard Compliance

PVCI compliant control port

- Data input and output handshake interfaces
- Supports 4:2:2 YCbYCr input format
- Different output formats (4:2:2, 4:2:0, 4:1:1, 4:1:0) possible by choosing from different scaling factors for luminance and chrominance components
- Support of cosited and non-cosited output formats via programmable phase offsets
- Discrete bypassing of each submodule is possible
- Output frame size for Main Picture Scaler (MRSZ) is up to 64 Mpixels.
- Output frame size for Self Picture Scaler (SRSZ) is independent from the Main Picture Scaler and is typically set to lower resolutions (e.g. Full HD). It can be object of customization.

The Resize module is configurable for horizontal and vertical up- or down-scaling.

Discrete values for the scaling factors of the luminance and the two chrominance components allow conversion between YUV4:2:2 and YUV4:2:0 color format and support of uneven line width.

Phase shift registers are provided to shift the output pixel positions with respect to the input pixel positions. This allows for e.g. format conversion between cosited and non-cosited color schemes.

In sensor mode the MRSZ block supports only down-scaling. This is because the sensor cannot be stopped from delivering data during one frame.

The Resize module is able to process luminance and chrominance data independently, i.e. there are separate pipelines for luminance and chrominance processing using dedicated scale factors and phase offsets. This allows format conversion to be done by the Resize block (YCbCr 4:2:2 to 4:2:0, 4:1:1, 4:1:0).

31.3.8 JPEG Encoder

The JPEG Encoder consists of the Raster-2-Block converter and the JPEG encoder core. It accepts YCbCr 4:2:2 data only.

The Raster-2-Block converter uses an optimized addressing algorithm for its block memory, so that a total of 8 line buffers are sufficient. The block memory operates in a limited way as a FIFO, so some delay in the processing behind the Raster-2-Block converter can be leveled.

The data input interface is a 16 bit YCbCr 4:2:2 interface. As the encoder core accepts 8 bit data only, the Raster-2-Block converter accepts 16 bit pixel data at maximum half the clock speed, i.e. after taking a 16 bit sample it de-asserts its acknowledge for one clock cycle.

The output interface is 64 bits wide. Both interfaces use handshaking. The programming interface is a 16 bit PVCI interface.

31.3.9 YC_bC_r to RGB Conversion

In the self-picture path a YCbCr to RGB conversion unit is present to provide display-ready image data for LCD displays. The image data is stored in one memory region of the system memory. These formats are supported: RGB 888 with 24 bit per pixel, RGB 666 with 18 bit per pixel and RGB 565 with 16 bit per pixel.

The conversion from YCbCr 4:2:2 to 4:4:4 mode is performed by storing the chrominance value of the previous pixel. Thus a set of Y, Cb and Cr values is available for every pixel to be processed. These values are used to generate an RGB value for the pixel by using the following formulas for 8 bit (0 – 255) RGB, assuming a nominal range of 16 to 235 for luminance and 16 to 240 for chrominance values:

R = 1,164*(Y - 16) + 1,596*(Cr - 128)

G = 1,164*(Y - 16) - 0,813*(Cr - 128) - 0,391*(Cb - 128)

B = 1,164*(Y - 16) + 2,018*(Cb - 128)

The result is forwarded to the MI as 24 bit word via the sp_y_data port, the chroma port (sp_c_data) is inactive in this case.

The module can be configured to support RGB 565 and RGB 666 by clipping the RGB 888 values. In case of RGB 565 only the lower 16 bits of the data port to the SP_Y_FIFO are used. In bypass mode (no RGB conversion) the conversion functionality is inactive and the incoming luminance and chrominance values are simply fed through to the MI. See the following Figure for the memory organization for the self picture path:

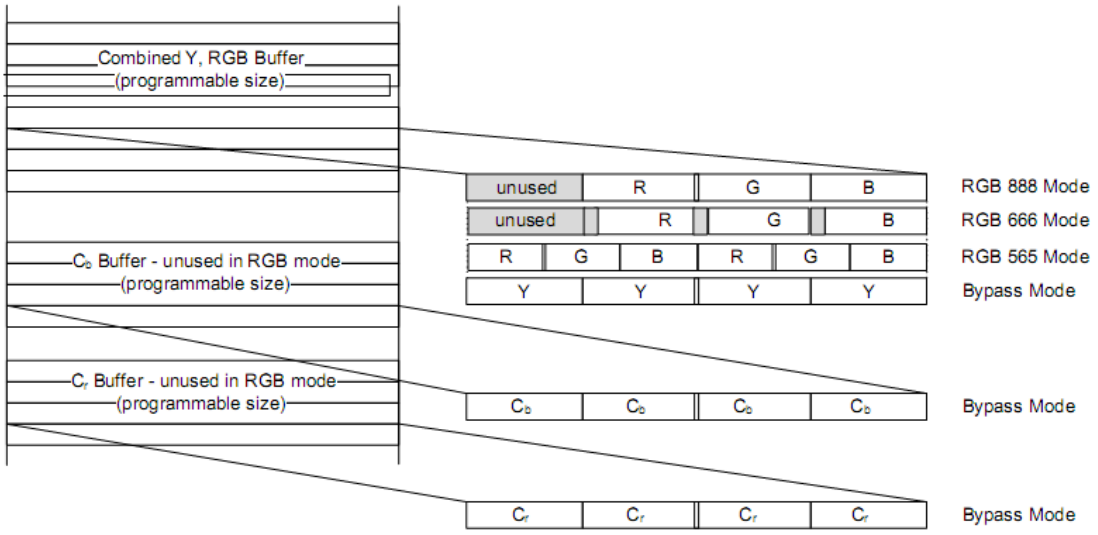

Fig. 31-3 Memory Organization for the Self Picture Path

31.3.10 Memory Interface (MI)

The Memory Interface block provides three data bus master ports to the system memory, two write ports and one read port.

Write Port

The Memory Interface is responsible for collecting the internal data streams and writing them into system memory. Therefore it is attached to data bus master wrappers to access (write) the system bus.

The following types of data streams are supported:

- Raw 8 or 12 bit data
- 64 bit JPEG data
- 2x 8 bit Y, Cb/Cr main image data
- 2x 8 bit Y, Cb/Cr self-picture data

The following modes of operation must be supported:

- Raw data only
- JPEG data only
- Main image data only
- Self-picture data only
- Parallel main image and self-picture data
- Self-picture and JPEG data
- Semi-planar mode

The image data has to be split into Y, Cb and Cr data to be separately written into system memory. So the Memory Interface (write port) consists of six FIFOs for the data.

The FIFOs are necessary for the component separated data streams of main and self-picture data path. Some of the FIFOs have to be re-used for the raw data and JPEG data stream. See Fig.25-4 for the definition of memory buffers and Fig.25-5 for the storage scheme in planar and semi-planar mode.

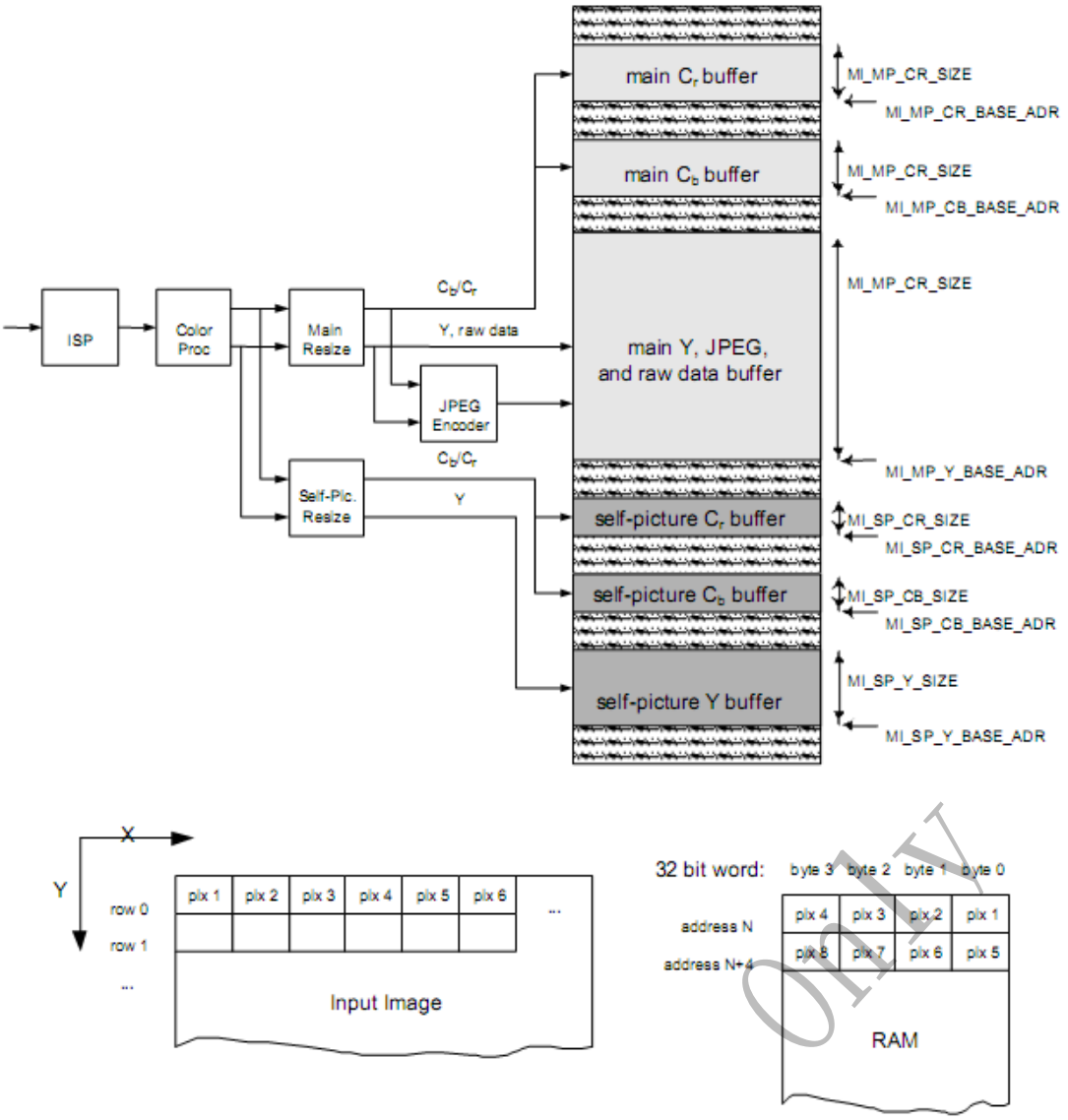

Fig. 31-4 Definition of Memory Buffers

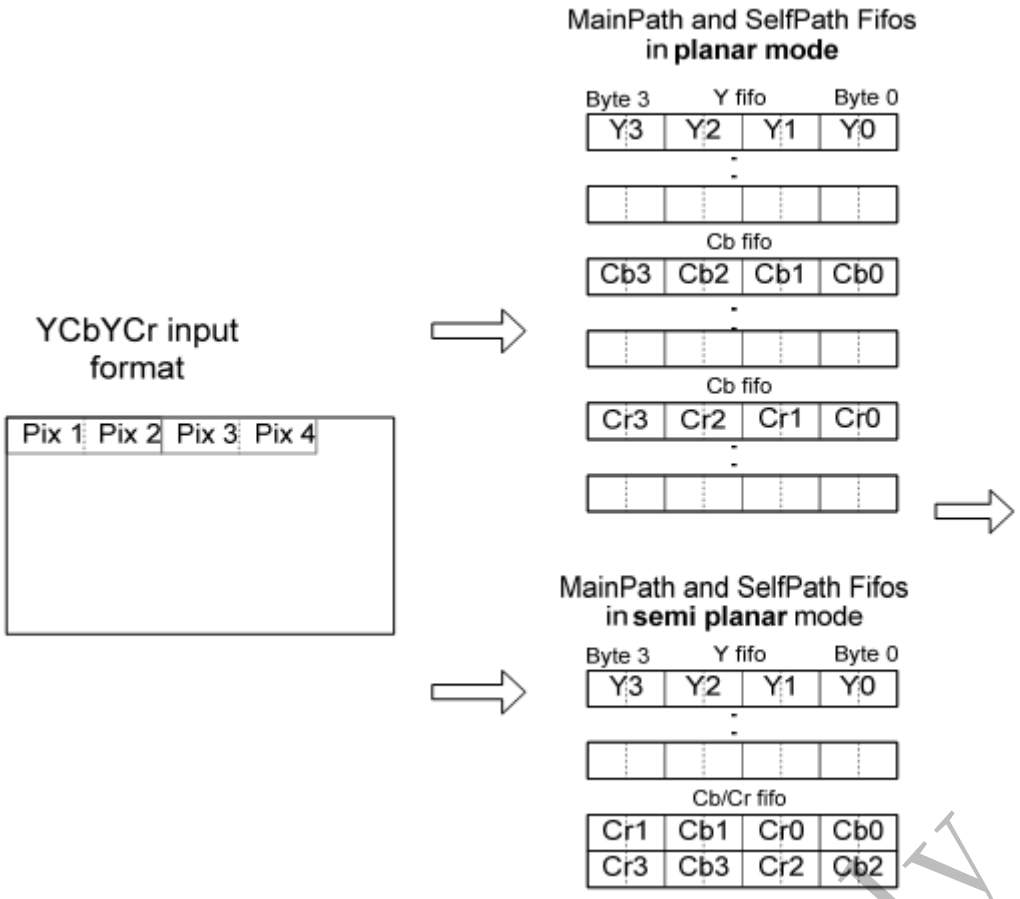

Fig. 31-5 Storage Scheme in Planar and Semi-planar Mode

Read port (DMA)

The Memory Interface also supports reading back picture data from the system memory.

Therefore it is attached to a second data bus master wrapper to access (read) the system data bus.

Three independent read channels are provided to accommodate the three color components of a picture. The picture has to be stored component separated (planar) in system memory. If one or two components are not used they can be turned off by programming the respective component size to zero. So it's also possible to read back raw or JPEG data through one single channel.

The Memory Interface (read port) consists of three FIFOs, one FIFO per channel. Each FIFO features a PVCI interface at the output, so data can be easily halted by de-asserting the acknowledge line.

31.3.11 Control Unit

The Control Unit serves two purposes:

1. Interface o the local configuration register blocks of the other modules

2. Clock and reset control registers for ISP Controller core

The Control Unit has one 32 bit PVCI input interface and multiple 32 bit PVCI output interfaces. All transfers from the PVCI input interface are 32 bit wide.

Each block inside the ISP Controller IP core uses a dedicated clock signal that can be controlled by a programming register inside the Control Unit.

Existing software resets in the ISP Controller blocks can also be controlled by a programming register inside the Control Unit. An asynchronous reset for the processing clock domain has to be generated from the system reset. A soft reset for all registers in the IP core is provided. It works like an asynchronous reset.

All sub module processing clocks can be switched on and off. All sub module configuration clocks are enabled only when the dedicated address is active. All gated processing and configuration clocks are phase synchronous to the processing clock.

31.4 Register Description

The ISP uses a distributed configuration register scheme. So there is no central unit containing all programming registers, but all sub-modules contain their own programming registers. An address space is reserved for each sub-module inside the total ISP Controller address space.

31.4.1 Registers Summary

No.	Module	Description	Base Name	Offset Address
1	MX_main_control	ISP Main Control Registers	MRV_AFM_BASE	0x0000
2	MX_image_effects	Image Effects	MRV_IMGEFF_BASE	0x0200
3	MX_superimpose	Superimpose	MRV_SI_BASE	0x0300
4	MX_isp	ISP main registers	MRV_ISP_BASE	0x0400
5	MX_isp_flash	FLASH_LIGHT registers	MRV_FLASH_BASE	0x0660
6	MX_isp_shutter	SHUTTER registers	MRV_SHUT_BASE	0x0680
7	MX_cproc	COLOR PROCESSING registers	MRV_CPROC_BASE	0x0800
8	MX_main_resize	MAIN RESIZE registers	MRV_MRSZ_BASE	0x0c00
9	MX_self_resize	SELF RESIZE registers	MRV_SRSZ_BASE	0x1000
10	MX_mi	Memory Interface registers	MRV_MI_BASE	0x1400
11	MX_jpeg	JPEG ENCODER registers	MRV_JPE_BASE	0x1800
12	MX_smia	SMIA Interface registers	MRV_SMIA_BASE	0x1a00
13	MX_mipi	MIPI Interface registers	MRV_MIPI_BASE	0x1c00
14	MX_isp_afm	ISP Auto Focus Measurement	MRV_AFM_BASE	0x2000

No.	Module	Description	Base Name	Offset Address
15	MX_isp_lsc	ISP Lens Shade Correction	MRV_LSC_BASE	0x2200
16	MX_isp_is	ISP Image Stabilization	MRV_IS_BASE	0x2300
17	MX_isp_hist	ISP Histogram	MRV_HIST_BASE	0x2400
18	MX_isp_filter	ISP Filter	MRV_FILT_BASE	0x2500
19	MX_isp_cac	ISP Chromatic Aberration Correction	MRV_CAC_BASE	0x2600
20	MX_isp_exposure	ISP Auto Exposure Measurement	MRV_AE_BASE	0x2700
21	MX_isp_bls	ISP Black Level Subtraction	MRV_BLS_BASE	0x2800
22	MX_isp_dpf	ISP De-noising Pre-filter	MRV_DPF_BASE	0x2900
23	MX_isp_dpcc	ISP Defect Pixel Cluster Correction	MRV_DPCC_BASE	0x2900
24	MX_isp_wdr	ISP Wide Dynamic Range	MRV_WDR_BASE	0x2a00

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

31.4.2 Detail Register Description

The description of the ISP register reference **5.1 Register Interface of CamerIC2D_user_manual_M14v2.pdf.**

31.5 Interface Description

Table 31-1 ISP Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
isp_clkin	I	CIFclkin_GPIO2b3	GPIO2B_IOMUX[7:6]= 2'b01
isp_href	I	CIFhref_GPIO2b2	GPIO2B_IOMUX[5:4]= 2'b01
isp_vsync	I	CIFvsync_GPIO2b1	GPIO2B_IOMUX[3:2]= 2'b01
isp_data0	I	CIFdata0_I2C3scl_cam_HDMIddc_scl_GPIO1d4	GPIO1D_IOMUX[9:8]= 2'b01
isp_data1	I	CIFdata1_I2C3sda_cam_HDMIddc_sda_GPIO1d5	GPIO1D_IOMUX[11:10]= 2'b01
isp_data2	I	CIFdata2_HSADCdata0_BBdebug0_GPIO2a0	GPIO2A_IOMUX[1:0]= 2'b01

isp_data3	I	CIFdata3_HSADCdata1_BBdebug1_GPIO2a1	GPIO2A_IOMUX[3:2]= 2'b01
isp_data4	I	CIFdata4_HSADCdata2_BBdebug2_GPIO2a2	GPIO2A_IOMUX[5:4]= 2'b01
isp_data5	I	CIFdata5_HSADCdata3_BBdebug3_GPIO2a3	GPIO2A_IOMUX[7:6]= 2'b01
isp_data6	I	CIFdata6_HSADCdata4_BBdebug4_GPIO2a4	GPIO2A_IOMUX[9:8]= 2'b01
isp_data7	I	CIFdata7_HSADCdata5_BBdebug5_GPIO2a5	GPIO2A_IOMUX[11:10]= 2'b01
isp_data8	I	CIFdata8_HSADCdata6_BBdebug6_GPIO2a6	GPIO2A_IOMUX[13:12]= 2'b01
isp_data9	I	CIFdata9_HSADCdata7_BBdebug7_GPIO2a7	GPIO2A_IOMUX[15:14]= 2'b01
isp_data01	I	CIFdata01_GPIO1d6	GPIO1D_IOMUX[13:12]= 2'b01
isp_data11	I	CIFdata11_GPIO1d7	GPIO1D_IOMUX[15:14]= 2'b01

Notes: 1. I=input, O=output, I/O=input/output, bidirectional

31.6 Application Notes

The description of the Application Notes reference **5.1 Register Interface of CamerIC2D_user_manual_M14v2.pdf.**