QN902X

Ultra Low Power BLE System-on-Chip Solution

Rev. 1.1 — 10 February 2015 Product data sheet

1. Introduction

QN902x is an ultra-low power wireless System-on-Chip (SoC) for Bluetooth Smart applications, supporting both master and slave modes. It integrates a high performance 2.4 GHz RF transceiver with a 32-bit ARM Cortex-M0 MCU, Flash memory, and analog and digital peripherals.

By integrating a Bluetooth v4.0 Low Energy compliant radio, link controller and host stack, QN902x provides a single chip solution for Bluetooth Smart applications. The 32-bit ARM Cortex-M0 MCU and on-chip memory provide additional signal processing and room to run applications for a true single-chip Bluetooth Smart solution. In addition, QN902x can also be utilized as a network processor by connecting to an application processor via UART or SPI to add Bluetooth Smart feature to any products.

QN902x comes with complete analog peripherals and digital interfaces to enable easy connection to any analog or digital peripherals or sensors, and external application processor in network processor mode.

2. General description

QN902x is an ultra-low power, high performance and highly integrated Bluetooth v4.0 Low Energy (BLE) solution for Bluetooth Smart applications such as sports/fitness, human interface devices, and app-enabled smart accessories. It is especially designed for wearable electronics and can run on small capacity battery such as a coin cell battery.

QN902x integrates a BLE radio, controller, protocol stack and profile software on a single chip, providing a flexible and easy to use BLE SoC solution. It also includes a high performance MCU and on-chip memory that can support users to develop a single-chip wireless MCU solution. Users can also utilize QN902x as a network processor by connecting to an application processor for more advanced applications.

Additional system features include fully integrated DC/DC and LDO, low power sleep timer, battery monitor, general purpose ADC, and GPIOs, to further reduce overall system cost and size. QN902x operates with a power supply range of 2.4 V to 3.6 V and has very low power consumption in all modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance.

3. Features and benefits

- True single-chip BLE SoC solution
  - Integrated BLE radio
  - Complete BLE protocol stack and application profiles
  - Support both master and slave modes
  - Up to 8 simultaneous links in master mode
- RF
  - -95 dBm RX sensitivity (non DC-DC mode)
  - -93 dBm RX sensitivity (DC-DC mode)
  - TX output power from -20 dBm to 4 dBm
  - Fast and reliable RSSI and channel quality indication
  - Compatible with worldwide radio frequency regulations
- Very low power consumption
  - Single 2.4 V to 3.6 V power supply
  - Integrated DC-DC and LDO
  - 2 µA deep sleep mode
  - 3 µA sleep mode (32 kHz RC OSC on)
  - 9.25 mA Rx current with DC-DC
  - 8.8 mA Tx current @0 dBm Tx power with DC-DC
- Compact 6x6 QFN48 and 5x5 QFN32 package
- Microcontroller
  - Integrated 32-bit ARM Cortex M0 MCU
  - 64 kB system memory
  - User controllable code protection
- High level integration
  - 4-channel 10-bit general purpose ADC
  - Two general purpose analog comparator
  - Up to 31 GPIO pins
  - GPIO pins can be used as interrupt sources
  - Four general purpose timers
  - 32 kHz sleep timer
  - Watchdog timer
  - Real time clock with calibration
  - 2-channel programmable PWM
  - Two SPI/UART interface
  - I2C master/slave interface
  - Brown-out Detector
  - Battery monitor
  - AES-128 security coprocessor
  - 16/32 MHz crystal oscillator
  - Low power 32 kHz RC oscillator
  - 32.768 kHz crystal oscillator

4. Applications

- Sports & Fitness
- Healthcare & medical
- Remote control
- Smartphone accessories
- PC peripherals (mouse, keyboard)
- Wireless Sensor networks

4.1 Profiles and Services

QN902x offers a complete list of qualified profiles and services.

Table 1. Supported profiles/services

Profiles/Services	Version
Device Information Service	1.1
Battery Service	1.0
Blood Pressure Profile	1.0
Find Me Profile	1.0
Glucose Profile	1.0
Heart Rate Profile	1.0
Health Thermometer Profile	1.0
HID over GATT Profile	1.0
Proximity Profile	1.0
Scan Parameter Profile	1.0
Time Profile	1.0
Alert Notification Profile	1.0
Phone Alert Status Profile	1.0
Cycling Speed and Cadence Profile	1.0
Running Speed and Cadence Profile	1.0

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
QN9020	QFN48	Plastic-Encapsulated 48-Pin Bluetooth Low Energy 4.0 SoC Chip; 6x6 mm Body	4.0
QN9021	QFN32	Plastic-Encapsulated 32-Pin Bluetooth Low Energy 4.0 SoC Chip; 5x5 mm Body	4.0

6. Block diagram

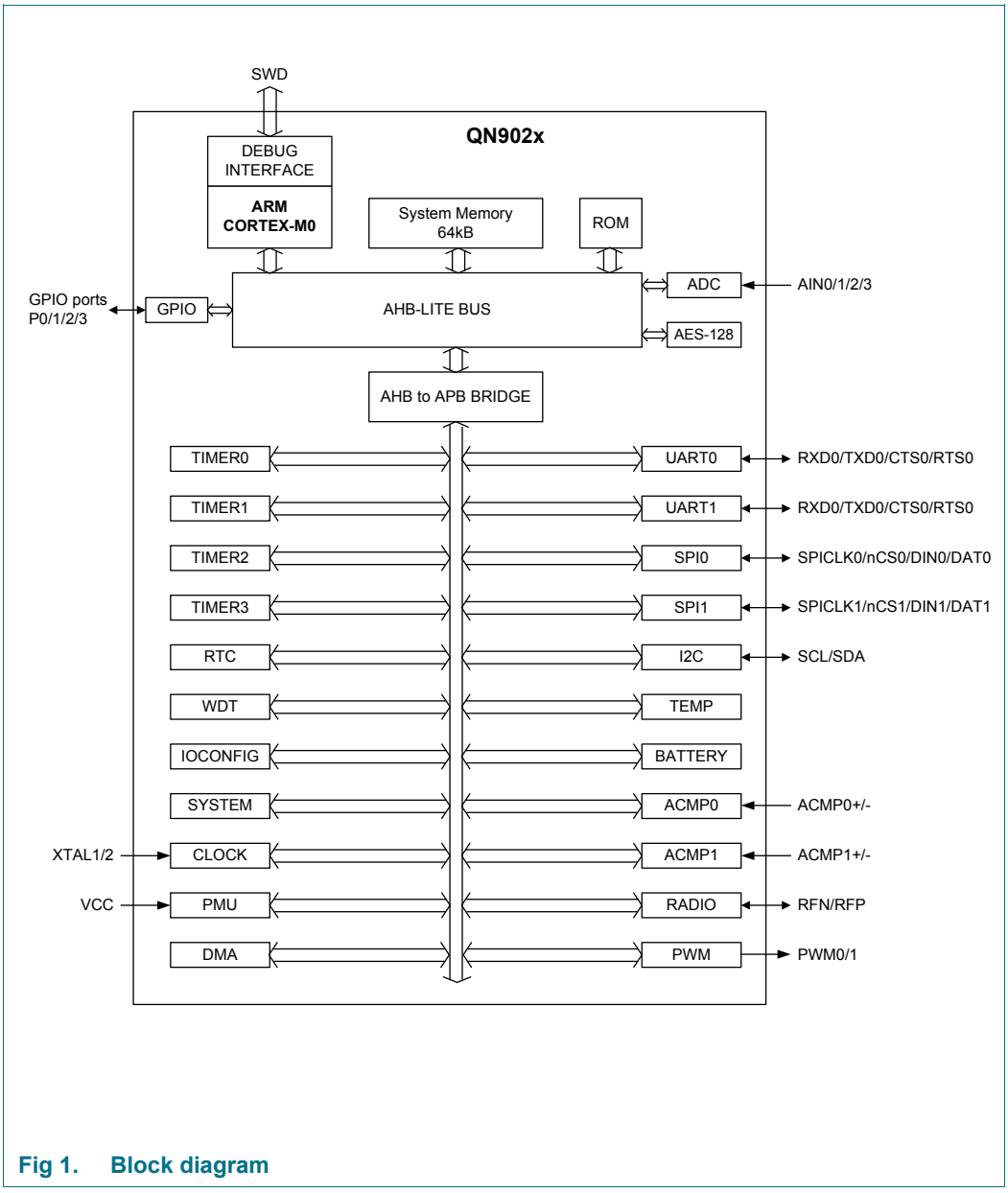
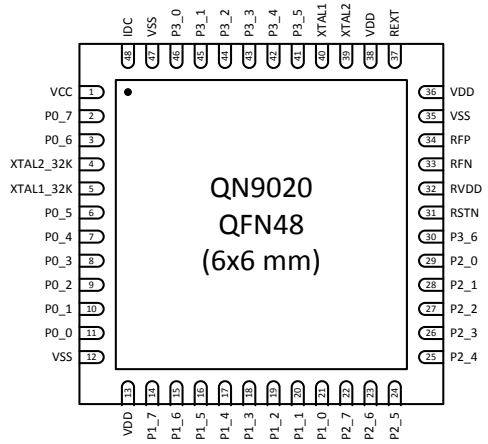


Fig 1. Block diagram

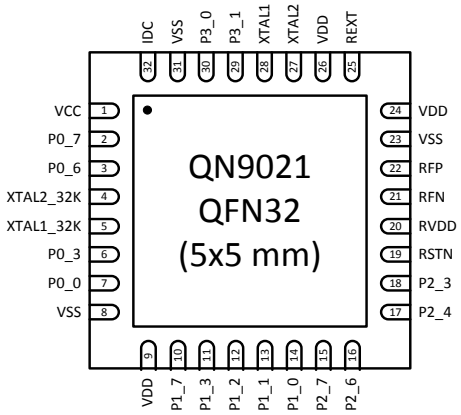
7. Pinning information for QN902x

7.1 Pinning



QN9020 is in a 6x6 mm QFN48 package. The back plate must be grounded to the application PCB in order to achieve optimal performance.

Fig 2. QN9020 Pin configuration



QN9021 is in a 5x5 mm QFN32 package. The back plate must be grounded to the application PCB in order to achieve optimal performance.

Fig 3. QN9021 Pin configuration

7.2 Pin description

Table 3. QN902x Pin description

Symbol	Pin		Alt Function	Description
	QN9020	QN9021		
V_{CC}	1	1		Power supply
P0_7	2	2	0: SWCLK (I) 1: P0_7 (I/O) 2: AIN3 (AI) 3: ACMP1- (AI)	SWCLK: Default to SWCLK (input with pull-up) P0_7: GPIO7 AIN3: ADC input channel 3 ACMP1-: Analog comparator 1 negative input
P0_6	3	3	0: SWDIO (I/O) 1: P0_6 (I/O) 2: AIN2 (AI) 3: ACMP1+ (AI)	SWDIO: Default to SWDIO (input with pull-up) P0_6: GPIO6 AIN2: ADC input channel 2 ACMP1+: Analog comparator 1 positive input
XTAL2_32K	4	4		Connected to 32.768 kHz crystal or external 32k clock. Unconnected if RC OSC used.
XTAL1_32K	5	5		Connected to 32.768 kHz crystal. Unconnected if RCOSC used.
P0_5	6		0: P0_5 (I/O) 1: SCL (I/O) 2: ADCT (I) 3: ACMP1_O (O)	P0_5: GPIO5 SCL: I2C clock ADCT: ADC conversion external trigger ACMP1_O: analog comparator result output
P0_4	7		0: P0_4 (I/O) 1: CLKOUT1(O) 2: RTCI(I)	P0_4: GPIO4 CLKOUT1: clock output 1 RTCI: RTC input capture
P0_3	8	6	0: P0_3 (I/O) 1: CLKOUT0 (O) 2: T0_ECLK (I/O)	P0_3: GPIO3 CLKOUT0: Clock output 0 T0_ECLK: Timer 0 external clock input or PWM output
P0_2	9		0: P0_2 (I/O) 1: SDA (I/O) 2: SPICLK0 (I/O) 3: RTS0 (O)	P0_2: GPIO2 SDA: I2C data transmit SPICLK0: SPI0 clock RTS0: UART0 RTS
P0_1	10		0: P0_1 (I/O) 1: nCS0_0(I/O) 2: CTS0 (I)	P0_1: GPIO1 nCS0_0: SPI0 slave select for master/slave mode CTS0: UART0 CTS
P0_0	11	7	0: P0_0 (I/O) 1: TXD0 (O) 2: DAT0 (I/O) 3: RTCI (I)	P0_0: GPIO0 TXD0: UART0 Tx data output with pull-up DAT0: In 4-wire mode, SPI0 output data. In 3-wire mode, data I/O RTCI: RTC input capture

Symbol	Pin		Alt Function	Description
	QN9020	QN9021		
VSS	12	8		Ground
VDD	13	9		Power supply
P1_7	14	10	0: P1_7 (I/O) 1: RXD0 (I) 2: DIN0 (I) 3: T0_0 (O)	P1_7: GPIO15 RXD0: UART0 Rx data input DIN0: SPI0 input data in 4-wire mode, invalid in 3-wire mode T0_0: Timer 0 PWM output
P1_6	15		0: P1_6 (I/O) 1: nCS0 _1 (O) 2: PWM0 (O) 3: T0_3 (I/O)	P1_6: GPIO14 nCS0_1: SPI0 slave select output for master mode PWM0: PWM0 output T0_3: Timer 0 input capture /clock or PWM output
P1_5	16		0: P1_5 (I/O) 1: PWM1 (O) 2: T1_2 (I/O)	P1_5: GPIO13 PWM1: PWM1 output T1_2: Timer 1 input capture /clock or PWM output
P1_4	17		0: P1_4 (I/O) 1: T1_3 (I/O)	P1_4: GPIO12 T1_3: Timer 1 input capture /clock or PWM output
P1_3	18	11	0: P1_3 (I/O) 1: SPICLK1 (I/O) 2: RTS1 (O) 3: CLKOUT1 (O)	P1_3: GPIO11 SPICLK1: SPI1 clock RTS1: UART1 RTS CLKOUT1: Clock output 1
P1_2	19	12	0: P1_2 (I/O) 1: nCS1_0 (I/O) 2: CTS1 (I) 3: ADCT (AI)	P1_2: GPIO10 nCS1_0: SPI1 slave select for master/slave mode CTS1: UART1 CTS ADCT: ADC conversion external trigger
P1_1	20	13	0: P1_1 (I/O) 1: DAT1 (I/O) 2: TXD1 (O) 3: T1_0 (I/O)	P1_1: GPIO9 DA1: In 4-wire mode, SPI1 output data. In 3-wire mode, data I/O TXD1: UART1 Tx data T1_0: Timer 1 input capture /clock or PWM output
P1_0	21	14	0: P1_0 (I/O) 1: DIN1 (I) 2: RXD1 (I) 3: T2_ECLK (I/O)	P1_0: GPIO8. DIN1: SPI1 input data in 4-wire mode, invalid in 3-wire mode RXD1: UART1 Rx data T2_ECLK: Timer 2 external clock input or PWM output
P2_7	22	15	0: P2_7 (I/O) 1: ACMP1_O (O) 2: PWM0 (O) 3: T1_ECLK (I/O)	P2_7: GPIO23. ACMP1_O: Analog comparator result output PWM0: PWM0 output T1_ECLK: Timer 1 external clock input or PWM output

Symbol	Pin		Alt Function	Description
	QN9020	QN9021		
P2_6	23	16	0: P2_6 (I/O) 1: PWM1 (O) 2: T2_0 (I/O)	P2_6: GPIO22. PWM1: PWM1 output T2_0: Timer 2 input capture /clock or PWM output
P2_5	24		0: P2_5 (I/O) 1: nCS1_1 (O) 2: T2_2 (I/O)	P2_5: GPIO21. nCS1_1: SPI1 slave select output for master mode T2_2: Timer 2 input capture /clock or PWM output
P2_4	25	17	0: P2_4 (I/O) 1: SCL (I/O) 2: PWM1 (O) 3: T3_ECLK (I/O)	P2_4: GPIO20. SCL: I2C master clock output with pull-up PWM1: PWM1 output T3_ECLK: Timer 3 external clock input or PWM output
P2_3	26	18	0: P2_3 (I/O) 1: SDA (I/O) 2: ACMP0_O (O) 3: T3_0 (I/O)	P2_3: GPIO19. SDA: I2C data transmit ACMP0_O: Analog comparator result output T3_0: Timer 3 input capture /clock or PWM output
P2_2	27		0: P2_2 (I/O) 1: SPICLK1 (I/O) 2: RTS1 (O) 3: T2_3 (I/O)	P2_2: GPIO18. SPICLK1: SPI1 clock RTS1: UART1 RTS T2_3: Timer 2 input capture /clock or PWM output
P2_1	28		0: P2_1 1: DAT1 (I/O) 2: TXD1 (O) 3: T3_1 (I/O)	P2_1: GPIO17. DAT1: In 4-wire mode, SPI0 output data. In 3-wire mode, data I/O TXD1: UART1 Tx data output with pull-up T3_1: Timer 3 input capture /clock or PWM output
P2_0	29		0: P2_0 (I/O) 1: DIN1 (I) 2: RXD1 (I) 3: T3_2 (I/O)	P2_0: GPIO16 DIN1: SPI1 input data in 4-wire mode, invalid in 3-wire mode RXD1: UART1 Rx data input T3_2: Timer 3 input capture /clock or PWM output
P3_6	30		0: P3_6 (I/O) 1: nCS1_0 (I/O) 2: CTS1 (I)	P3_6: GPIO30 nCS1_0: SPI1 slave select for master/slave mode CTS1: UART1 CTS
RSTN	31	19		Hardware reset, active low
RVDD	32	20		Regulated PA power output.
RF_N	33	21		Differential RF port
RF_P	34	22		Differential RF port
VSS	35	23		Analog ground
VDD	36	24		Analog power supply

Symbol	Pin		Alt Function	Description
	QN9020	QN9021		
REXT	37	25		Current reference terminal Connect 56 kΩ ±1% resistor to ground.
AVDD	38	26		Analog power supply
XTAL2	39	27		Connected to 16 MHz or 32 MHz crystal or external clock
XTAL1	40	28		Connected to 16 MHz or 32 MHz crystal. Unconnected if external clock used.
P3_5	41		0: P3_5 (I/O) 1: nCS0_0 (I/O) 2: T0_0 (I/O)	P3_5: GPIO29 nCS0_0: SPI0 slave select for master/slave mode T0_0: Timer 0 input capture /clock or PWM output
P3_4	42		0: P3_4 (I/O) 1: SPICLK0 (I/O)	P3_4: GPIO28 SPICLK0: SPI0 clock
P3_3	43		0: P3_3 (I/O) 1: DAT0 (I/O) 2: CLKOUT0 (O)	P3_3: GPIO27 DAT0: In 4-wire mode, SPI0 output data. In 3-wire mode, data I/O CLKOUT0: Clock output 0
P3_2	44		0: P3_2 (I/O) 1: DIN0 (I) 2: ACMP0_O (O)	P3_2: GPIO26 DIN0: SPI0input data in 4-wire mode, invalid in 3-wire mode ACMP0_O: Analog comparator result output
P3_1	45	29	0: P3_1 (I/O) 1: T0_2 (I/O) 2: AIN1 (I) 3: ACMP0- (I)	P3_1: GPIO25 T0_2: Timer 0 input capture /clock or PWM output AIN1: ADC input channel 1 ACMP0-: Analog comparator negative input
P3_0	46	30	0: P3_0 (I/O) 1: T2_1 (I/O) 2: AIN0 (AI) 3: ACMP0+ (AI)	P3_0: GPIO24. T2_1: Timer 1 input capture /clock or PWM output AIN0: ADC input channel 0 ACMP0+: Analog comparator positive input
VSS	47	31		Ground
IDC	48	32		PWM driver for LC filter if DC/DC is enabled. If the DC/DC is disabled, this pin shall not be connected.

8. Functional diagram

QN902x integrates an ultra-low power 2.4 GHz radio, qualified software stack and application profiles on a single chip. The integrated Power Management Unit (PMU) controls the system operation in different power states to ensure low power operation. The high frequency crystal oscillator provides the reference frequency for the radio transceiver, while the low frequency oscillators maintain timing in sleep states.

The integrated AES coprocessor supports encryption/decryption with minimal MCU usage to offload MCU and reduce power consumption. The embedded MCU and

additional memory provide additional signal processing capability and run user applications.

QN902x includes a general purpose ADC with four external independent input channels. The ADC can be utilized for power supply voltage monitoring. Digital serial interfaces (SPI/UART/I2C) are integrated to communicate with application processor or digital sensors.

The UART supports the Bluetooth Low Energy Direct Test Mode (DTM).This interface is used to control the PHY layer with commercially available Bluetooth testers used for qualification.

I2C is integrated and support both master and slave mode. It can communicate with digital sensor or EEPROM.

8.1 MCU Subsystems

The MCU subsystem includes

- 32-bit ARM Cortex-M0 MCU
- 64 kB system memory
- Reset generation
- Clock and power management unit
- Nested Vectored Interrupt Controller (NVIC)

Serial Wire Debug interface (SWD)

8.1.1 MCU

The CPU core is a 32-bit ARM Cortex-M0 MCU, which offers significant benefits to application development, including:

- Simple, easy-to-use programmers model
- Highly efficient ultra-low power operation
- Excellent code density
- Deterministic, high-performance interrupt handling for 32 external interrupt inputs

The processor is extensively optimized for low power, and delivers exceptional power efficiency through its efficient instruction set, providing high-end processing hardware including a single-cycle multiplier.

8.1.2 Memory organization

QN902x integrates on-chip 64 kB system memory for application program and data. The system memory, all registers and external devices are allocated in the same memory map within 4 GB, ranging from 0x00000000 to 0xFFFFFFFF, which is shown in Fig 4. The system memory security is ensured with a user controllable protection scheme, preventing un-authorized read out.

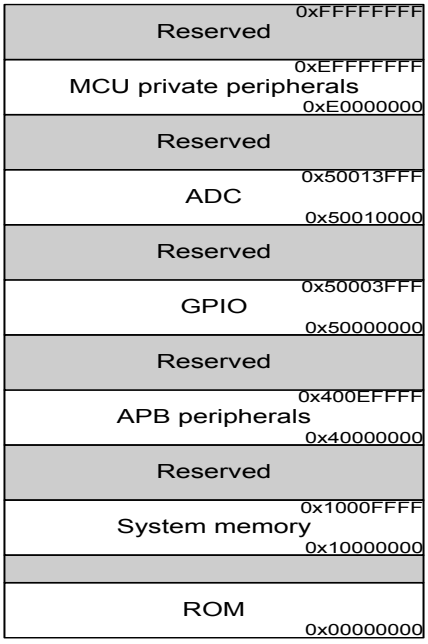


Fig 4. Memory address map

8.1.3 RESET generation

The device has four reset sources. The following events generate a reset:

- Forcing RSTN pin low
- Power-on reset
- Brown-out reset
- Watchdog timeout reset

8.1.4 Nested Vectored Interrupt Controller (NVIC)

QN9020 supports Cortext-M0 built-in Nested Vectored Interrupt Controller (NVIC) with 24 external interrupt inputs. External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and Cortex-M0 processor core are closely coupled, providing low-latency interrupt processing and efficient processing of late arriving interrupts.

8.1.5 Clock and power management

QN902x provides flexible clocking scheme to balance between performance and power. A high frequency crystal oscillator is utilized to provide reference frequency and system clock, which supports 16/32 MHz external crystal with ±50 ppm accuracy. The system clock could be 32 MHz or its divided versions.

Two low speed 32 kHz oscillators are integrated. The 32.768 kHz crystal oscillator is used where accurate timing is needed, while 32 kHz RC OSC could reduce cost and power consumption. Only one can work at any one time.

QN902x features ultra-low power consumption with two sleep modes, SLEEP and DEEP SLEEP. After execution of Wait for Interrupt (WFI) instruction, the MCU stops execution, enters into sleep mode and stops the clock immediately. If DEEP SLEEP mode is entered, it must wait for external interrupts to wake it up. Before entering into SLEEP mode, MCU should set the sleep timer correctly and make the 32 kHz clock ready.

Once an interrupt (external interrupt or sleep timer timeout) occurs, the Wakeup Interrupt Controller (WIC) enables the system clock, takes a number of clock cycles to wake up MCU and restore the states, before MCU can resume program execution to process the interrupt.

Only P0_0 to P0_7 and P1_0 to P1_7 can wakeup MCU out of sleep states. The power management unit is responsible to control the power states of the whole chip and switch on/off the supply to different parts according to the power state

Table 4. Power matrix

Mode	Digital Regulator	32kHz OSC	Sleep timer	Note
Deep sleep	Off	Off	Off	Wait external interrupt to wake it up. RAM/register content retained
Sleep	Off	On	On	Wait for SLEEP TIMER timeout to wake it up. RAM/register content retained
Idle	On	On	On	16/32 MHz XTAL on. MCU idle.
Active	On	On	On	Radio off, MCU on
Radio	On	On	On	Radio on.

8.1.6 Serial Wire Debug (SWD) interface

QN902x provides a standard SWD interface and supports up to four hardware breakpoints and two watch points.

8.2 Flash

QN9020/1 have a 128K bytes flash. The flash communicates with MCU by internal SPI interface and can be used to store code or data. The flash has below functions:

- 32 Equal Sectors with 4K byte each. Any Sector can be erased individually
- Minimum 100,000 erase/program cycles
- RES command, 1-byte Command code
- Low Power Consumption

8.3 Digital Peripherals

8.3.1 TIMER (0/1)

TIMER0/1 are general-purpose 32-bit timer with programmable 10-bit prescaler. The prescaler source could be the system clock, 32 kHz clock or an external clock input. The timers have below functions:

- Input capture function
- Compare function
- PWM output

The timer generates maskable interrupts for the events of overflow, compare and capture, which could be used to trigger MCU or ADC conversions.

8.3.2 TIMER (2/3)

TIMER2/3 are general-purpose 16-bit timer with programmable 10-bit prescaler. The prescaler source could be the system clock, 32 kHz clock or an external input. The timers have below functions:

- Input capture function
- Compare function
- PWM output

The timer will generate maskable interrupts for the events of overflow, compare and capture, which could be used to trigger MCU or ADC conversions.

8.3.3 Real Time Clock (RTC)

The RTC is run off the 32 kHz clock and provides real time with calibration, supporting below functions:

- Time and date configuration on the fly
- Alarm function for 24-hour and minute
- Input capture function with programmable noise canceller

8.3.4 Watchdog Timer (WDT)

The Watchdog timer (WDT) is a 16-bit timer clocked by 32 kHz clock. It is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT resets the system when software fails to clear the WDT within the selected time interval. The WDT is configured as either a Watchdog Timer or as a timer for general-purpose use. If the watchdog function is not needed in an application, it is possible to configure the Watchdog Timer to be used as an interval timer that can be used to generate interrupts at selected time intervals. The maximum timeout interval is 1.5 days.

8.3.5 Sleep Timer

The sleep timer is a 32-bit timer running at 32 kHz clock rate. It is in always-on power domain, being used to set the interval for system to exit Sleep mode and wakeup MCU.

8.3.6 PWM

The PWM provides two channel PWM waveforms with programmable period and duty cycle. It has two 8-bit auto reload down counter and programmable 10-bit prescaler for both channels. It supports the functions mentioned below:

- Predictable PWM initial output state
- Buffered compare register and polarity register to ensure correct PWM output
- Programmable overflow interrupt generation

8.3.7 DMA

The DMA controller is used to relieve MCU of handling data transfer operations to achieve high performance and efficiency. It has a single DMA channel to support fixed and undefined length transfer. The source address and destination address are programmable. It can be aborted immediately in a transfer process by configuring ABORT register, and a DMA done interrupt is generated meanwhile.

8.3.8 Random number generator

QN902x integrates a random number generator for security purpose.

8.3.9 AES coprocessor

The Advanced Encryption Standard (AES) coprocessor allows encryption/decryption to be performed with minimal CPU usage. The coprocessor supports 128-bit key and DMA transfer trigger capability.

8.4 Communication Interfaces

8.4.1 UART 0/1

The two UARTs have identical function and include the following features:

- 8-bit payload mode: 8-bit data without parity
- 9-bit payload mode: 8-bit data plus parity
- The parity in 9-bit mode is odd or even configurable
- Configurable start- and stop- bit levels
- Configurable LSB- or MSB- first data transfer
- Parity and framing error status
- Configurable hardware flow control
- Support overrun
- Flexible baud rate: 1.2 / 2.4 / 4.8 / 9.6 / 14.4 / 19.2 / 28.8 / 38.4 / 57.6 / 76.8 / 115.2 / 230.4 kbps

8.4.2 SPI 0/1

The two SPIs have identical function and include the following features:

- Master/slave mode configurable

- 4-wire or 3-wire configurable
- Clock speed configurable for master mode (divided from AHB clock)
- 4 MHz max. clock speed in slave mode when AHB clock is 32 MHz
- 16 MHz max. clock speed in master mode when AHB clock is 32 MHz
- Configurable clock polarity and phase
- Configurable LSB or MSB first transfer

8.4.3 I2C

The I2C module provides an interface between the device and I2C-compatible devices connected by the 2-wire I2C serial bus. The I2C module features include:

- Compliance with the I2C specification v2.1
- 7-bit device addressing modes
- Standard mode up to 100 kbps and fast mode up to 400 kbps support
- Support master arbitration in master mode
- Support line stretch in slave mode

8.5 Radio and Analog Peripherals

8.5.1 RF transceiver

QN902x radio transceiver is compliant with the Bluetooth v4.0 Low Energy specification Volume 6, Part A. The transceiver requires a 32 MHz or 16 MHz crystal to provide reference frequency and a matching network to match an antenna connected to the receiver/ transmitter pins.

8.5.2 On-chip oscillators

QN902x includes three integrated oscillators:

- HFXO: Low power high frequency crystal oscillator supporting 32MHz or 16 MHz external crystal.
- LFXO: Ultra-low power 32.768 kHz crystal oscillator
- LFRCO: Ultra-low power 32 kHz RC oscillator with ±250 ppm frequency accuracy after calibration

The high frequency crystal oscillator provides the reference frequency for the radio transceiver. The low frequency 32.768 kHz oscillators provide the protocol timing. The low-frequency clock can also be obtained from a 32.768 kHz external clock source.
For HFXO, the external capacitance is integrated to reduce BOM cost. The capacitance can be adjusted by software.

8.5.3 DC/DC converter

QN902x includes highly efficient integrated regulators to generate all internal supply voltages from a single external supply voltage. Optional integrated DC-DC down converter can be utilized to further reduce the current consumption by 30%. This is particularly useful for applications using battery technologies with higher nominal cell voltages.

8.5.4 General purpose ADC

QN902x integrates a general purpose 8/10-bit SAR ADC, with up to 50k sampling rate. It includes an analog multiplexer with up to four external input channels. Conversion results can be moved to memory through DMA.

The main features of the ADC are as follows:

- Four single-end input channels, or two differential channels
- Reference voltage selectable as internal, external single-ended, AVDD
- Interrupt request generation
- DMA triggers at end of conversions
- Window compare function
- Battery measurement capability

The ADC could operates in

- Single conversion mode
- Continuous conversion mode
- Scan mode (automatic switching among external inputs)

8.5.5 Analog comparator

The analog comparator is used to compare the voltage of two analog inputs and a digital output to indicate the higher input voltage. The positive input is always from external pin, and the negative input can either be one of the selectable internal references or from external pin.

The analog comparator features for low-power operation and the comparing result can be used as interrupt source to wake up the system from sleep.

8.5.6 Battery monitor

A battery monitor is integrated by connecting supply voltage ($V_{DD}/4$) to the ADC input, which would use the internal regulated reference for the conversion.

9. Limiting values

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	V_{CC} to GND	-0.3	5.0	V
V_{DD}	Supply voltage	V_{DD} to GND	-0.3	5.0	V
T_s	Storage temperature		-55	+150	°C
ESD	Human-body model	RFN, RFP		1.5	kV
		Other pads		2	kV
	Machine model	RFN, RFP		100	V
		Other pads		200	V
	Charged-device model	All pads		1	kV

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Power supply	Relative to GND	2.4	3.0	3.6	V
V_{DD}	Power supply	Relative to GND	2.4	3.0	3.6	V
T_A	Operating temperature		-40	+25	+85	°C

11. Characteristics

11.1 DC Characteristics

Table 7. DC Characteristics

Typical values are T_A = 25 °C and V_{CC}/V_{DD} = 3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Icc	Current consumption	Deep sleep mode		2		µA
		Sleep mode		3		µA
		Idle mode (w/o DC-DC)		0.84		mA
		MCU @8 MHz (w/o DC-DC)		1.35		mA
		Rx mode(w/o DC-DC)		13.6		mA
		Rx mode (w/t DC-DC)		9.25		mA
		Tx mode @0 dBm Tx power (w/o DC-DC)		13.3		mA
		Tx mode @0 dBm Tx power (w/t DC-DC)		8.8		mA
Interface						
V_{OH}	High level output voltage		0.9*V_{CC}			V
V_{OL}	Low level output voltage				0.1*V_{CC}	V
V_{IH}	High level input voltage		0.7*V_{CC}			V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage				0.3*V_{CC}	V

Notes:

1. Current include current for both analog and digital.
2. Depend on IO conditions.
3. Deep sleep mode: digital regulator off, no clocks, POR, RAM/register content retained.
4. Sleep mode: digital regulator off, 32 kHz RC OSC on, POR, sleep timer on, and RAM/register content retained.
5. Idle: 16 MHz OSC on, no radio or peripherals, 8 MHz system clock and MCU idle (no code execution).
6. MCU@8 MHz: MCU running at 8 MHz RC OSC clock, no radio or peripherals.
7. Rx sensitivity is -95 dBm sensitivity when DC-DC is disabled.
8. Rx sensitivity is -93 dBm sensitivity when DC-DC is enabled.

Table 8. 16/32MHz Crystal Oscillator Reference Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{XTAL-MHz}$	Crystal frequency			16 or 32		MHz
Δf	Crystal accuracy requirement		-50		50	ppm
C_L	Crystal load capacitance		8		20	pF
	Start-up time (16 MHz)[1]				0.7	ms
	Start-up time (32 MHz)[1]				0.4	ms

[1] Guaranteed by design

Table 9. 32kHz Crystal Oscillator Reference Clock

Typical values are T_A = 25 ˚C and V_{CC}/V_{DD} = 3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{XTAL-32K}$	32k Crystal frequency			32.768		kHz
Δf	32k Crystal tolerance			250		ppm
C_L	Crystal load capacitance			12		pF
	Start-up time			1		s
$F_{RC-32kHz}$	32k RC oscillator frequency			32		kHz
$F_{RC-32kHz}$	32k RC clock accuracy after calibration			±0.1		%
	Temperature coefficient			0.04		% / ℃
	Supply-voltage coefficient			3		% / V
	Calibration time				1	ms

Table 10. RF receiver characteristics

Typical values are T_A = 25˚C and V_{CC}/V_{DD} = 3 V, f_c = 2440 MHz, BER<0.1%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Rx sensitivity (high performance mode)			-95		dBm
	Rx sensitivity(low power mode, w/t DC-DC)			-93		dBm
	Maximum input signal level			0		dBm
	Co-channel rejection(C/I)			6		dB
	Adjacent-channel rejection(C/I)	±1 MHz		-1		dB
	Alternate-channel rejection(C/I)	±2 MHz		-40		dB
	Image rejection (C/I_{imag})			-19		dB
	Out of band blocking 30 to 2000 MHz			-18		dBm
	Out of band blocking 2003 to 2399 MHz			-18		dBm
	Out of band blocking 2484 to 2997 MHz			-18		dBm
	Out of band blocking 3 to 12.75 GHz			-18		dBm

Table 11. RF transmitter characteristics

Typical values are T_A = 25 °C and V_{CC}/V_{DD} = 3 V, f_c=2440 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F	Frequency range		2400		2483.5	MHz
P_{TX}	Output power		-20		4	dBm
	Tx power adjust step			2		dB

Table 12. ADC characteristics

Typical values are T_A = 25 °C and V_{CC}/V_{DD} = 3 V, with differential ADC input signal

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Input voltage range	Single-ended	0		VREF	V
		Differential input	-VREF		VREF	V
ENOB	Effective Number of Bits	10-bit		9.3		bits
SNR	Signal to Noise Ratio	10-bit		59.3		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SFDR	Spur-Free Dynamic Range	10-bit		65.2		dB
THD	Total Harmonic Distortion	10-bit		-63		dB
DNL	Differential Nonlinearity	10-bit	-1	0.6	2	LSB
INL	Integral Nonlinearity	10-bit	-2	0.88	3	LSB
	Conversion time	10-bit		18		µs
	Gain Error	10-bit		4	10	LSB
	Offset	10-bit			2	LSB
	Current consumption – ADC	@1 MHz ADC clock		50	65	µA
	Current consumption - Buffer	@1 MHz ADC clock		140	180	µA
	Current consumption – PGA	@1 MHz ADC clock		90	120	µA

Table 13. Battery monitor characteristics

Typical values are T_A = 25 °C and V_{CC}/V_{DD} = 3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Battery monitor range		2.4		3.6	V
	Battery monitor accuracy			0.2		mV

Table 14. Analog comparator characteristics

Typical values are T_A = 25 °C and V_{CC}/V_{DD} = 3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
	Current consumption			0.3		µA
	Hysteresis			40		mV

12. Application information

12.1 Schematic for QN9020 with DC-DC Converter

A typical application schematic for QN9020 with DC-DC converter is shown in Fig 5.

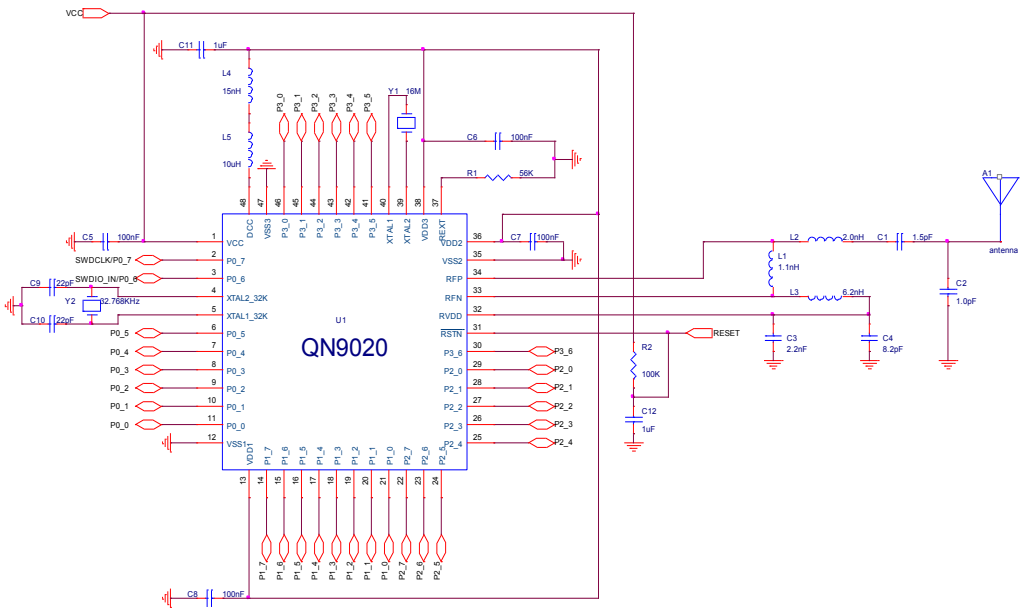


Fig 5. QN9020 Typical application schematic with DC-DC converter

For application using battery supply, it is highly recommended to apply the circuit for QN9020 with internal DC-DC converter.

12.2 Schematic for QN9020 without DC-DC Converter

To use QN9020 without DC-DC converter, please follow the schematic in Fig 6 to use LDO regulator only.

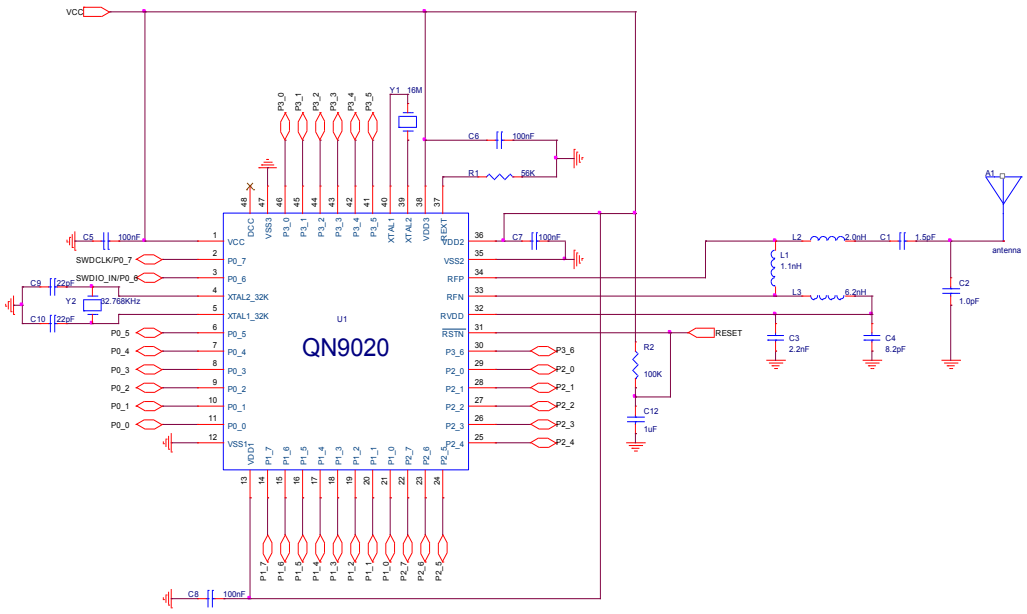


Fig 6. QN9020 Typical application schematic without DC-DC converter

12.3 Schematic for QN9021 with DC-DC Converter

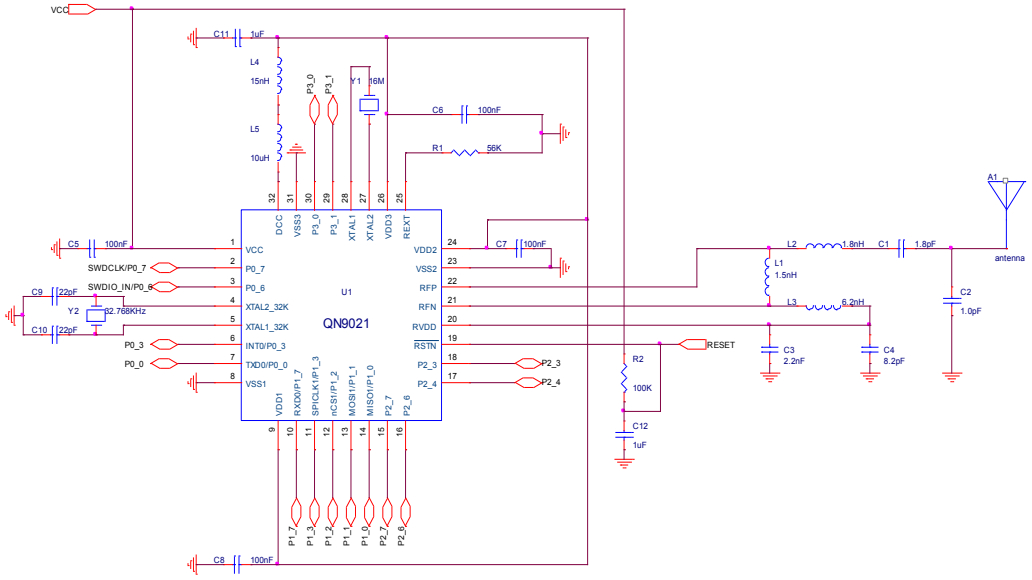


Fig 7. QN9021 Typical application schematic with DC-DC converter

For application using battery supply, it is highly recommended to apply the circuit for QN9021 with internal DC-DC converter.

12.4 Schematic for QN9021 without DC-DC Converter

To use QN9021 without DC-DC converter, please follow the schematic in Fig 8 to use LDO regulator only.

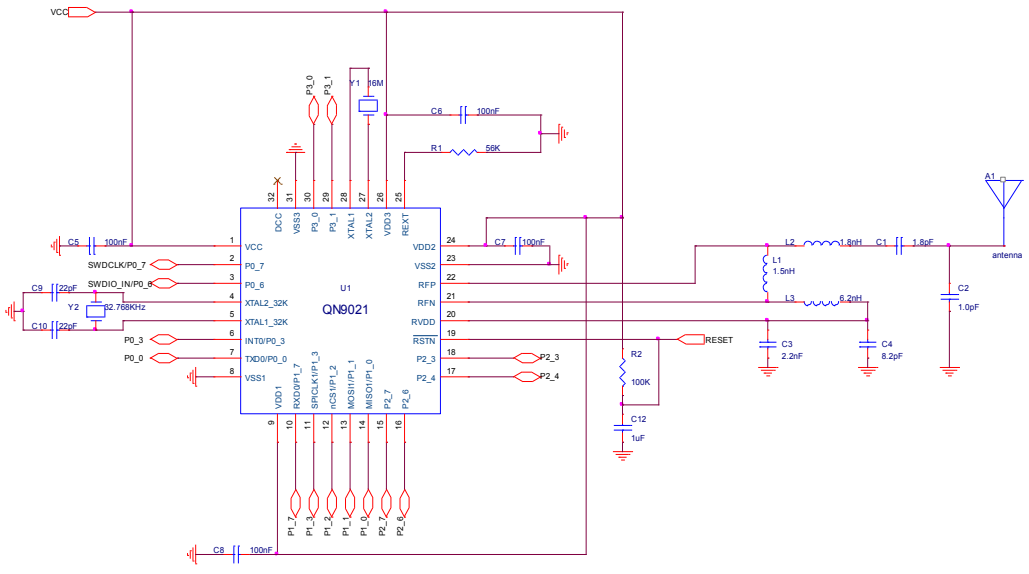


Fig 8. QN9021 Typical application schematic without DC-DC converter

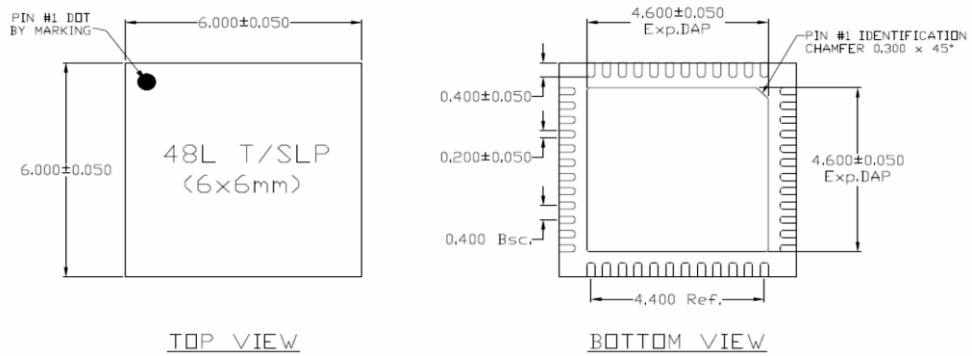
12.5 QN902x External Components List

Table 15. Internal circuits

Component	Description	Value
C5, C6, C7, C8	Supply Decoupling Capacitors	C_SMD, 100 nF, X5R, ±10%, 6.3 V, 0402
C11	Supply Decoupling Capacitors	C_SMD, 1 µF, NP0, ±5%, 6.3 V, 0402
C12	Capacitor used for reset	C_SMD, 1 µF, NP0, ±5%, 6.3 V, 0402
C9, C10	Crystal Loading Capacitors	C_SMD, 22 pF, NP0, ±5%, 25 V, 0402
R1	Resistor used for current reference	R_SMD,56K, ±1%, 0402
R2	Resistor used for reset	R_SMD, 100K, ±1%, 0402
L4	Chip Inductor for DC-DC	15 nH
L5	Chip Inductor for DC-DC	10 µH
L3	Inductor for RF matching network	6.2 nH
L1	Inductor for RF matching network	1.1 nH (QN9020) / 1.5 nH (QN9021)
L2	Inductor for RF matching network	2.0 nH (QN9020) / 1.8 nH (QN9021)
C3	Capacitor for RF matching network	2.2 nF
C4	Capacitor for RF matching network	8.2 pF
C1	Capacitor for RF matching network	1.5 pF (QN9020) / 1.8 pF (QN9021)
C2	Capacitor for RF matching network	1.0 pF
C13	Supply Decoupling Capacitor	C_SMD, 100 nF, X5R, ±10%, 6.3 V, 0402

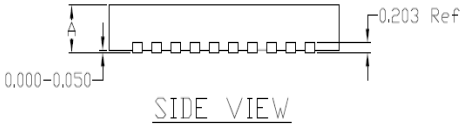
13. Package outline

13.1 QN9020 Package description



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

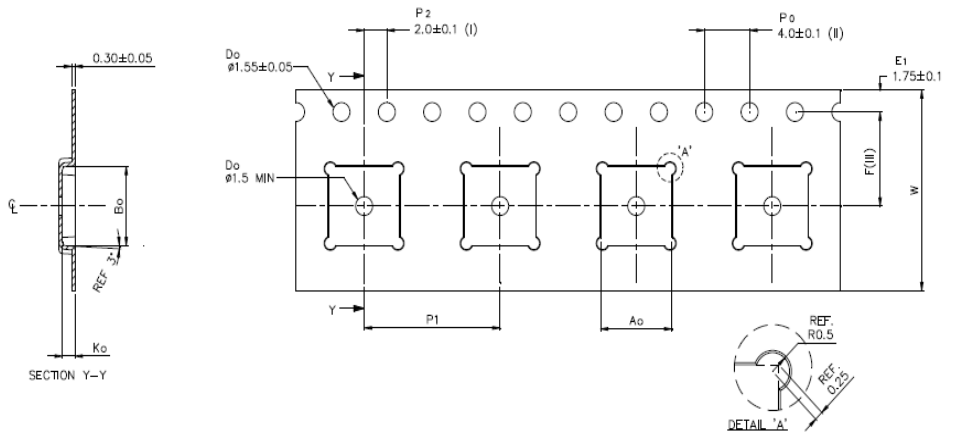


Note:

1. Only SLP is available
2. 48-Lead plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN]

Fig 9. QN9020 Mechanical drawing

Carrier Tape Dimensions



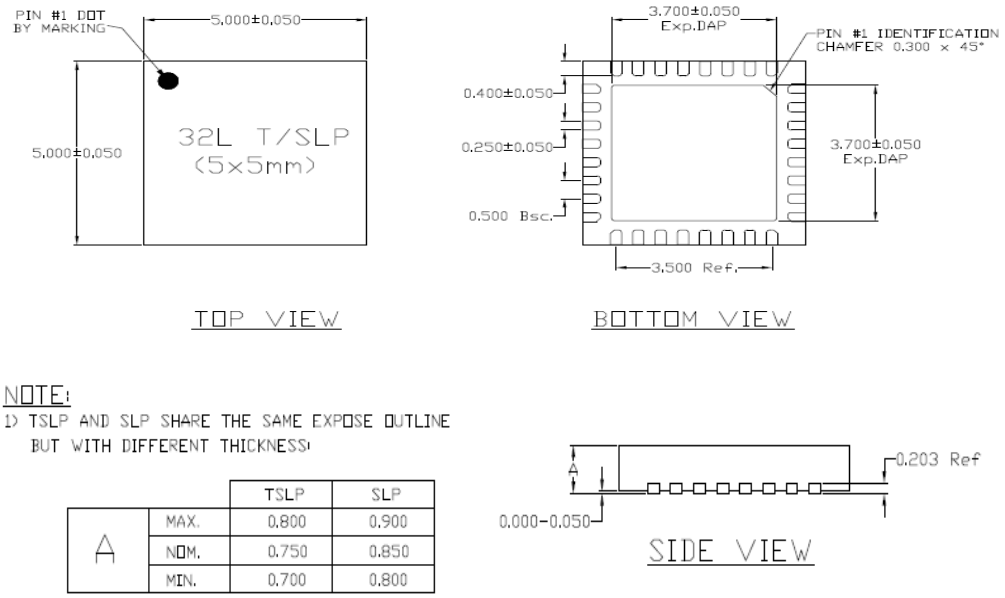
Note:

1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is +U0.20
3.

Ao	6.30 +/−0.1
Bo	6.30 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Fig 10. QN9020 Carrier tape dimensions

13.2 QN9021 Package Description



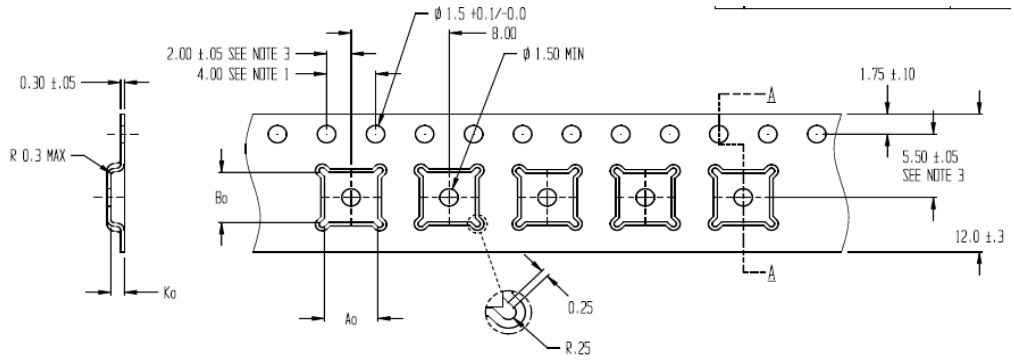
		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Note:

1. Only SLP is available
2. 32-Lead plastic Quad Flat, No Lead Package (ML) – 5x5 mm Body [QFN]]

Fig 11. QN9021 Mechanical drawing

Carrier Tape Dimensions



Note:

1. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
2. Cumulative tolerance of 10 sprocket holes is +U0.20.
3. Ao = 5.25
   Bo = 5.25
   Ko = 1.10

Fig 12. QN9021 Carrier tape dimensions

14. Soldering

14.1 Package Peak Reflow Temperature

QN902x is assembled in a lead-free QFN48 package and QFN32 package. Since the geometrical size of QN9020 is 6×6× 0.85 mm, and the geometrical size of QN9021 is 5×5× 0.85 mm, the volume and thickness is in the category of volume < 350 mm^3 and thickness < 1.6 mm in Table 4-2 of IPC/JEDEC J-STD-020C. The peak reflow temperature is:

$$T_p = 260^o C$$

The temperature tolerance is +0 ˚C and -5 ˚C. Temperature is measured at the top of the package.

14.2 Classification Reflow Profiles

Profile Feature		Specifications
Average Ramp-Up Rate (t_{smax} to t_P)		3 °C/s max.
Pre-heat:	Temperature Min (T_{smin})	150 °C
	Temperature Max (T_{smax})	200 °C
	Time (t_s)	60-180 s
Time maintained above:	Temperature (T_L)	217 °C
	Time (t_L)	60-150 s
Peak/Classification Temperature (T_p)		260 °C
Time within 5 °C of Actual Peak Temperature (t_p)		20-40 s
Ramp-Down Rate		6 °C/s max.
Time 25 °C to Peak Temperature		8 mins max.
Peak/Classification Temperature (T_p)		260 °C

Note:

1. All temperatures are measured at the top of the package.

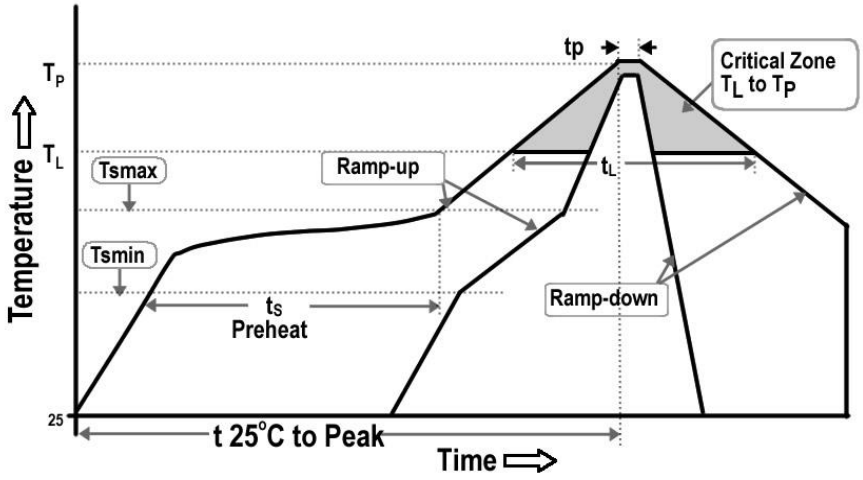


Fig 13. Reflow Temperature Profile

14.3 Maximum Reflow Times

All package reliability tests were performed and passed with a pre-condition procedure that repeat a reflow profile, which conforms to the requirements in Section 14.2, three (3) times.

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
QN902x	20150210	Product data sheet	-	

16. Legal information

16.1 Data sheet status

Document status[2][3]	Product status[4]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[2] Please consult the most recently issued document before initiating or completing a design.

[3] The term 'short data sheet' is explained in section "Definitions".

[4] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17. Contact information

For more information, please visit: http://www.nxp.com

18. List of figures

Fig 1. Block diagram 4
Fig 2. QN9020 Pin configuration 5
Fig 3. QN9021 Pin configuration 5
Fig 4. Memory address map 11
Fig 5. QN9020 Typical application schematic with DC-DC converter 21
Fig 6. QN9020 Typical application schematic without DC-DC converter 22
Fig 7. QN9021 Typical application schematic with DC-DC converter 23
Fig 8. QN9021 Typical application schematic without DC-DC converter 24
Fig 9. QN9020 Mechanical drawing 25
Fig 10. QN9020 Carrier tape dimensions 26
Fig 11. QN9021 Mechanical drawing 27
Fig 12. QN9021 Carrier tape dimensions 28
Fig 13. Reflow Temperature Profile 30

19. List of tables

Table 1. Supported profiles/services....3
Table 2. Ordering information....3
Table 3. QN902x Pin description....6
Table 4. Power matrix....12
Table 5. Absolute maximum ratings....17
Table 6. Operating conditions....17
Table 7. DC Characteristics....17
Table 8. 16/32MHz Crystal Oscillator Reference Clock 18
Table 9. 32kHz Crystal Oscillator Reference Clock....18
Table 10. RF receiver characteristics....19
Table 11. RF transmitter characteristics....19
Table 12. ADC characteristics....19
Table 13. Battery monitor characteristics....20
Table 14. Analog comparator characteristics....20
Table 15. Internal circuits....24
Table 16. Revision history....30

20. Contents

1. Introduction 1
2. General description 1
3. Features and benefits 2
4. Applications 3
4.1 Profiles and Services 3
5. Ordering information 3
6. Block diagram 4
7. Pinning information for QN902x 5
7.1 Pinning 5
7.2 Pin description 6
8. Functional diagram 9
8.1 MCU Subsystems 10
8.1.1 MCU 10
8.1.2 Memory organization 10
8.1.3 RESET generation 11
8.1.4 Nested Vectored Interrupt Controller (NVIC) 11
8.1.5 Clock and power management 11
8.1.6 Serial Wire Debug (SWD) interface 12
8.2 Flash 12
8.3 Digital Peripherals 13
8.3.1 TIMER (0/1) 13
8.3.2 TIMER (2/3) 13
8.3.3 Real Time Clock (RTC) 13
8.3.4 Watchdog Timer (WDT) 13
8.3.5 Sleep Timer 13
8.3.6 PWM 14
8.3.7 DMA 14
8.3.8 Random number generator 14
8.3.9 AES coprocessor 14
8.4 Communication Interfaces 14
8.4.1 UART 0/1 14
8.4.2 SPI 0/1 14
8.4.3 I2C 15
8.5 Radio and Analog Peripherals 15
8.5.1 RF transceiver 15
8.5.2 On-chip oscillators 15
8.5.3 DC/DC converter 15
8.5.4 General purpose ADC 16
8.5.5 Analog comparator 16
8.5.6 Battery monitor 16
9. Limiting values 17
10. Recommended operating conditions 17
11. Characteristics 17
11.1 DC Characteristics 17
12. Application information 21
12.1 Schematic for QN9020 with DC-DC Converter. 21
12.2 Schematic for QN9020 without DC-DC Converter 22
12.3 Schematic for QN9021 with DC-DC Converter. 23
12.4 Schematic for QN9021 without DC-DC Converter 24
12.5 QN902x External Components List 24
13. Package outline 25
13.1 QN9020 Package description 25
13.2 QN9021 Package Description 27
14. Soldering 29
14.1 Package Peak Reflow Temperature 29
14.2 Classification Reflow Profiles 29
14.3 Maximum Reflow Times 30
15. Revision history 30
16. Legal information 31
16.1 Data sheet status 31
16.2 Definitions 31
16.3 Disclaimers 31
17. Contact information 32
18. List of figures 33
19. List of tables 34
20. Contents 35

For more information, please visit: http://www.nxp.com

Date of release: 10 February 2015
Document identifier: QN902X